

ENEE 350
 TEST 1-Fall 2004-10/14/04
 CLOSED BOOK AND NOTES
 EXAM PERIOD: 75 MINUTES
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Instructions:

- A. Points for each problem are indicated right after the problem. The total score is 100 points.
- Use the space provided below each problem. if you need more space, please ask a proctor.
 - Write your name and student id on the cover sheet.
 - Promptly hand in your test to a proctor when the test is over.

NAME:

STUDENT ID:

Problem 1 (20 points):

- (a) Suppose that a processor executes instructions each of which is 16-bits long. How many different instructions can the instruction repertoire of this processor include if you assume that each instruction must be identified by a 4-bit opcode?
- (b) Suppose that only 7 instructions in the instruction repertoire of this processor require a 12-bit address, and all of its other instructions will execute operations on operands stored in a pair of registers (A and B) as in the **VESP** processor. Describe an instruction format that allows this processor to have 16 such instructions in addition to the 7 instructions that require a 12-bit address.

Problem 2 (20 points):

The computation engine of a given processor executes four shift instructions on a 4-bit operand,

$$A = [a_0, a_1, a_2, a_3]$$

whose instruction format is given below:

Instruction	Op-code	Shift direction	Number of shifts
SHL1	00	Left	1
SHL2	01	Left	2
SHR1	10	Right	1
SHR2	11	Right	2

Design a combinational circuit that can carry out these shift instructions in the computation engine of this processor. (*Note: You are required to describe only a combinational circuit that performs these shift instructions, not the entire computation engine of the processor.*)

Problem 3 (25 points): A useful instruction to include in a processor's repertoire is a move instruction that can index memory locations with a variable index displacement. The instruction format below describes one such instruction:

op-code	direction of move	source or destination address	index displacement
1111	1 bit	13 bits	6 bits

If the *direction of move* bit is 0 then the 13-bit address points to the destination of the operand and the address of the operand in the memory is found in the index register IX. If this bit is 1 then the 13-bit address points to the source of the operand and its destination address is found in the index register IX. In both cases, the

address in the index register is replaced by $IX + \text{index displacement}$, where the index displacement is a 6-bit signed number in 2's complement notation.

Assuming that this instruction has already been identified (decoded), describe its execution using an instruction register (IR), index register (IX), a memory address register (MAR), and a temporary register (TEMP). (You may assume that the memory (MEMORY) holds 24-bit instructions and data.)

Problem 4 (20 points): A given processor has four operand registers A, B, C, and D in addition to a program counter (PC), an instruction register (IR), memory address register, and memory data register, MDR. The following sequence of steps describes the instruction fetch, decode, and execute steps of this CPU:

```
while(reset == 0)
{
  Step 1: MAR = PC; PC = PC + 1;
  Step 2: MDR = MEMORY[MAR];
  Step 3: IR = MDR;
  Step 4: switch(IR[0:1])
  {
    case 0: A = A + B; break;
    case 1: A = A - B; break;
    case 2: A = A + B + C + D; break;
    case 3: A = A + B - (C + D); break;
  }
}
```

Give a control (sequential) circuit that performs the instruction fetch-decode-execute sequence of this processor, clearly indicating the events that occur at each state of the circuit.

Problem 5 (15 points): Write a vesp program to change the signs of the three numbers stored in memory locations 120,121,122.

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