ENEE350
Sample Final
CLOSED BOOK AND NOTES
EXAM PERIOD 120 MINUTES

Instructions:

- Each problem is worth 5 points. No partial credits. The total score is 100 points + 5 bonus points.
- Use the space provided below each problem. if you need more space, please ask a proctor.
- Write your name and student id on the cover sheet.
- Promptly hand in your test to a proctor when the test is over.

NAME: _____

STUDENT ID: _____

Problem 1: Consider the following code where *x* is a 2-bit number and A is a 32-bit register:

```
if ( x == 0) A = A;
if ( x == 1) A = A  << 1;
if ( x == 2) A = A <<  2;
if ( x == 3) A = A <<  3;
```

If this code is implemented in hardware, what is the minimum number of clock cycles which is needed to shift A left 10 times?

(a) 1 clock cycle	(b) 4 clock cycles	(c) 8 clock cycles
(d) 2 clock cycles	(e) 3 clock cycles	

Problem 2: The instruction repertoire of a certain computer consists of 100 instructions each of which uses three memory operands. Operands are accessed by specifying an address in the memory. The result is stored in one of the operand locations. Assuming that the memory of this computer contains 1024 locations, and the operands can be accessed at any memory location, the minimum number of bits to code all the instructions is

(a) 38 bits	(b) 30 bits	(c) 37 bits
(d) 36 bits	(e) none of the above	

Problem 3: A certain computer uses a scratchpad with 8 registers, each holding 16 bits. If at least half of these registers must be set aside to strictly hold operands, what is the maximum number of memory locations which can be addressed by this computer using register adressing?

(a) 2^{16}	(b) 2^{32}	(c) 2^{48}
(d) 2^{64}	(e) none of the above	

Problem 4: Which of the following statements is true?

(a) Operands in memory can be accessed faster using direct addressing rather than indirect addressing.	(b) If a computer uses indirect addressing only, some memory locations cannot be accessed.	(c) Direct addressing makes it impossible to write a self-modifying code.
(d) Direct addressing leads to longer instruction words.	(e) none of the above.	

Problem 5: Suppose that *p,q*, and *r* are 16-bit 2's complement numbers. Computing the expression $8\times p + 32\times q - 4\times r$ on a processor which can add or subtract two 16-bit numbers in 1 clock cycle and shift a 16-bit number one bit to the left or to the right in 1 clock cycle, will take

(a) 5 clock cycles	(b) 12 clock cycles	(c) 4 clock cycles
(d) 10 clock cycles	(e) none of the above	

Problem 6: A stack program that computes the in-order expression 3 + (2 – 6 – (4 – 7)) is

(a) PUS 3; PUS 7; PUS 5; PUS 2; SUS; SUS; SUS;	(b) PUS 5; PUS 2; SUS; PUS 7; SUS; PUS 3; SUS;	(c) PUS 2; PUS 5; SUS; PUS 7; SUS; PUS 3; SUS;
(d) (a) and (c)	(e) all of the above.	

Problem 7: An in-order expression for the post-order expression, pq+2uv-p+-q-+ is

(a) p+ q + (u-v)+p - 2 –q	(b) p+ q + (u-v)+p - 2 –q	(c) 2-[(u-v)+p] –q + (p+q)
(d) 2-[(u-v)+p] +q - (p+q)	(e) none of the above.	

Problem 8: The fetch-decode-execute cycle of a processor is shown below:

```
while (reset == 0) {MAR = PC; PC = PC + 1; read = 1; IR = RAM[MAR];
                    switch(IR)
                    {case 0: R0= R0 + R1;break; case 1: R0= R0 - R1;  break;
                     case 2: R0= R0 | R1; break;  case 3: R0= R0&R1; break;
                    }
                   }
```

How many clock cycles does the fetch-decode-execute cycle take?

(a) 1	(b) 2	(c) 3
(d) 4	(e) 5	

The binary codes for the vesp instructions are given below in hexadecimal notation:

ADD: 0, CMP: 1, LDA: 2, MOV: 3, JMP: 4, JEZ: 5, JPS: 6, HLT: 7, INC: 8, DEC: 9, AND: A, IOR: B, SHL: C, SHR: D, MXF: E, MXT: F.

Problem 9: What will be the decimal value stored in the A register after the following vesp program, which is written in hexadecimal notation, is executed? (All the numbers are in hexadecimal format)

Location 100: 2000 Location 101: 0010 Location 102: 3001 Location 103: 0101
Location 104: 1000 Location 105: 0000 Location 106: 8000 Location 107: 7000

(a) 16	(b) 0	(c) 24
(d) 32	(e) none of the above.	

Problem 10: What will be decimal value of the PC after the following vesp program is executed? (Locations are shown in decimal format)

Location 100: 2000 Location 101: 0010
Location 102: 606A Location 103: 7000
Location 104: 1000 Location 105: 7000
Location 106: 6068 Location 107: 7000

(a) 103	(b) 105	(c) 107
(d) 106	(e) none of the above.	

A microprogrammed processor uses the following 16-bit microinstruction format and operations:

ABUS select	BBUS select	OBUS	Destination	Branch condition	Branch address
1 bits	1 bit	3 bits	3 bits	2 bits	6 bits

ABUS select	Code	BBUS select	Code	OBUS	Code	Destination select	Code
A	0	B	0	ABUS	000	A	000
IR	1	MDR	1	BBUS	001	B	001
				ABUS + BBUS	010	MDR	010
				ABUS + ~BBUS + 1	011	PC	011
				~ABUS	100	IR	100
				~BBUS	101	IX	101
				1	110	MAR	110
				0	111		

Branch condition	Code
A>0	00
A=0	01
0	10
1	11

Problem 11: Which of the following microprograms (written in hexadecimal) performs the computation: A = A - B;

(a) 1880	(b) 2080	(c) 18C0
(d) 20C0	(e) none of the above.	

Problem 12: Which of the following micro-operations cannot be performed on this microprogrammed processor?

(a) MAR = MDR	(b) IR = MDR	(c) A = A + MDR
(d) A = 0;	(e) none of the above.	

Problem 13: What will be the decimal value stored in the A register after the following microprogram (written in hexadecimal) is executed?

location 0: 3080 location 1: 3180
location 2: 50C4 location 3: 1080
location 4: 5880

(a) 1	(b) 0	(c) 4
(d) 2	(e) none of the above.	

Problem 14: A processor executes two instructions in the time it fetches and decodes one instruction. If it takes 10^{-9} seconds to fetch and decode an instruction, and if the speed of the execution unit is doubled, how many seconds will it take to fetch-decode and execute an instruction on this processor?

(a) 1.75×10^{-8}	(b) 1.5×10^{-9}	(c) 1.25×10^{-9}
(d) 1.33×10^{-9}	(e) none of the above.	

Problem 15: A computer is designed as a cascade of A, B, C, and D units. Its operations are carried out by cycling through each of these four units repetitively where all units carry their part of the computation in the same amount of time. If A,B, and C can be speeded up without any limit, but D cannot be speeded up at all, what will be maximum speed up that this computer can have?

(a) 1	(b) 2	(c) 4
(d) 3	(e) none of the above.	

Problem 16: The following blocks of memory are cached into a 4-frame cache from left to right using the least recently used replacement algorithm. What four blocks of memory will reside in the cache after the last block is referenced? 8 7 4 1 2 8 6 5 8 1 2 1 3

(a) 1,5,6,8	(b) 1,2,3,5	(c) 1,2,3,8
(d) 1,2,3	(e) none of the above.	

Problem 17: A set associative cache memory uses 2 sets of 4 frames each to hold blocks of 256 words which are loaded from a memory of 16,384 words. How many blocks will be assigned to each set?

(a) 128	(b) 32	(c) 64
(d) 16	(e) none of the above.	

Problem 18: An interrupt service circuit uses a dynamic algorithm to adjust the priorities of two devices *x,y* that can interrupt a computer. Each time it examines the interrupt requests, the circuit services the devices as follows:

(1) If no device has interrupted, nothing is done,

(2) If only one device has interrupted, that device is serviced, and the priorities are left unchanged,

(3) If two devices have interrupted the device that has interrupted with high priority is serviced and the priorities of the two devices are switched.

Assuming that *x* is assigned the high priority (priority 1), *y* is assigned low priority (priority 2) when the circuit begins first its operation, which of the following sequences of services are rendered for the sequence interrupt requests x, xy, xy,x,xy,xy,xy,y,x?

(a) x,x,y,x,y,x,x,y,x	(b) x,x,y,x,x,y,x,y,x	(c) x,x,y,x,x,y,x,x,y
(d) x,y,x,x,y,y,x,y,x	(e) none of the above.	

Problem 19: A 5-stage arithmetic pipeline is clocked at 4 GHz where each stage uses 2 clock cycles. How many seconds will it take to execute 100 add instructions?

(a) 25×10^{-9}	(b) 26×10^{-9}	(c) 52×10^{-9}
(d) 50×10^{-9}	(e) none of the above.	

Problem 20: Suppose that a 6-stage instruction pipeline executes a mix of programs that contains 20% conditional branch instructions. Assume that all stages take one cycle. If every conditional branch instruction stalls (delays) the pipeline by 1 cycle to determine if the branch should be taken and no other instruction stalls it, how much speed-up would this pipeline provide in executing the given mix of programs over a serial processor?

(a) 4	(b) 6	(c) 3
(d) 5	(e) none of the above.	

Problem 21: Write a multiple choice problem which covers your favorite material in the course, and mark the correct answer. (without using any of the problems in the test.)

Have a great summer!