Accuracy of CMOS-Based Piezoresistive Stress Sensor for Engineering Applications of Thermal Loading Condition: Theoretical Review and Experimental Validation

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***Abstract*— Measurement uncertainties of a CMOS-based piezoresistive stress sensor are studied for low cycle thermal loading applications. After the fundamentals of the sensor are reviewed briefly, the random uncertainties associated with the data acquisition unit are evaluated first using raw current signals obtained from uniquely fabricated free-standing stress sensor chips. The free-standing sensor chips are tested further for systematic uncertainties associated with the manufacturing-induced residual stresses by subjecting them to a thermal cycle. Finally, the stress measurement accuracy of the sensor chip under an in-situ thermal loading is quantified by a numerical model verified by a sub-micron sensitivity optical technique while incorporating the quantified uncertainties.**

***Index Terms*— Piezoresistive stress sensor, uncertainty, prognostics and health management.**

I. Introduction

THE piezoresistive stress sensors were developed to measure directly the stresses of a silicon chip embedded in a semiconductor package. The concept of a resistance-based sensor was first introduced in 1961 [1], and later it was implemented for semiconductor packaging applications [2], [3]. The resistance-based sensors are typically fabricated in a relatively large scale ($\approx$ 300 μm by 300 μm). The measured stress value represents an average stress over the sensor area, and thus quantitative measurements of critical stresses is challenging. In addition, the resistive stress sensors require a reference measurement for a stress-free state. These reference measurements have to be repeated at all temperatures of interest [3], which makes the implementation for manufacturing problems virtually impractical.

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The CMOS (Complementary Metal-Oxide Semiconductor)-based stress sensor was developed to cope with the limitations of the resistance-based sensor [4]. It can be fabricated in a much smaller scale (a typical single measurement cell of 50 μm by 50 μm), which enables the sensor to detect a local stress concentration. By placing transistors in a current mirror configuration, the calibration is no longer required for the CMOS-based sensor. Additional benefits include: (1) the measurement system becomes simpler as the output signal is an electric current that can be measured directly; (2) it is easy to integrate the sensor with active circuitries; (3) multiplexers are readily implementable, which allows simultaneous data acquisition from all measurement cells; and (4) the sensitivity is enhanced because a lightly doped silicon is used to fabricate the sensor.

The CMOS-based stress sensor was implemented by various research groups, most notably, by Jaeger *et al.* [5]–[7]. They analyzed the behavior of the CMOS-based stress sensor in various measurement circuits and selected a cascade current mirror configuration to investigate the effect of encapsulation process on the package stress. A research group of Freiburg University IMTEK designed a CMOS-based stress sensor, which used the pseudo hall effect in silicon. They characterized the sensor [8], [9], created the matrix of cells with active circuitries [10]–[12], and utilized it to monitor the wire bonding process [13], [14].

More recently, the sensor was considered for prognostics and health management (PHM). In [15]–[17], Roberts et al. studied the evolution of stresses during packaging processes and thermal cycling reliability testing. They found that the stress changed rapidly at the beginning of cycling, but had only small changes afterwards. In [18], Rahim *et al.* showed the changes in stress sensor signal caused by delamination and warpage failure. Similar results during thermal cycling were presented by Shindler-Saefkow *et al.* [19] and Chang *et al.* [20], [21]. In [22] and [23], Lall *et al.* observed the changes in stresses measured by the sensor before delamination occurred, which was identified as a possible leading indicator of failure. In Ref. [24]–[29], various prognostics attempts were made using the stress sensor for the PHM of automotive electronics, including the internal stress measurement of molded electronic control units and the in-situ failure or fault detection.

Some considerations about the measurement accuracy of the resistance-based sensor, associated with calibration errors and rosette alignment errors, can be found in the literature [2], [30], but only limited information is available for the accuracy of the CMOS-based sensor, in particular the accuracy during thermal excursions, which are the primary application of interest to the authors. In order to extend its applicability further into actual applications in the PHM domain of electronics, it is imperative to assess quantitatively the uncertainties associated with the stress measurements using the advanced CMOS-based sensor. This is the motivation of the paper.

The objective of this paper is, thus, to quantify the measurement uncertainties of the advanced CMOS-based stress sensor and to provide the engineering guidelines for PHM applications. The fundamentals of the CMOS-based sensor are reviewed in Section II. The sensor chip and the data acquisition unit are described in Section III. The uncertainties of the stresses of free-standing sensors are discussed in Section IV. In Section V, a uniquely verified predictive numerical model is used to evaluate the measurement accuracy of the stresses of the sensor chip mounted on a ceramic substrate which is subjected to a thermal excursion.

II. Fundamentals of CMOS-Based Stress Sensor

Let us consider a coordination system shown in Figure 1, where the x and y axes are aligned with [110] and [$\bar{1}$00] crystallographic axes of silicon, respectively. The resistivity in the directions shown in Figure 1 can be described by the following set of equations [3]:

$$\left.\frac{\Delta\rho}{\rho}\right|_{0^\circ}^{90^\circ} = \frac{\pi_S^p}{2}(\sigma_{11}+\sigma_{22}) \mp \frac{\pi_{44}^p}{2}(\sigma_{11}-\sigma_{22}) + \pi_{12}^p\sigma_{33} + f_p(\Delta T) \quad (1)$$

$$\left.\frac{\Delta\rho}{\rho}\right|_{45^\circ}^{-45^\circ} = \frac{\pi_S^n}{2}(\sigma_{11}+\sigma_{22}) \mp \pi_D^n\sigma_{12} + \pi_{12}^n\sigma_{33} + f_n(\Delta T) \quad (2)$$

where ρ is the directional resistivity of silicon, π^p is the piezoresistive coefficient of p doped silicon, π^n is the piezoresistive coefficient of n doped silicon, $\pi_S = \pi_{11} + \pi_{22}$, $\pi_D = \pi_{11} - \pi_{22}$ and $f(\Delta T)$ is a function describing the effect of temperature on resistivity. In anisotropic piezoresistive materials, the relationship between the relative variation of resistivity ρ and mechanical stresses σ is described by the fourth-order tensor of the piezoresistive coefficients. Due to the cubic symmetry of the silicon crystal, the piezoresistive tensor Π related to the crystal directions [100], [010] and [001] contains only three independent quantities π_{11}, π_{12} and π_{44}.

The drain current of a Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) in the saturation region can be described by the following well-known equation [1]:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (3)$$

where:

V_{GS} - voltage between gate and source;

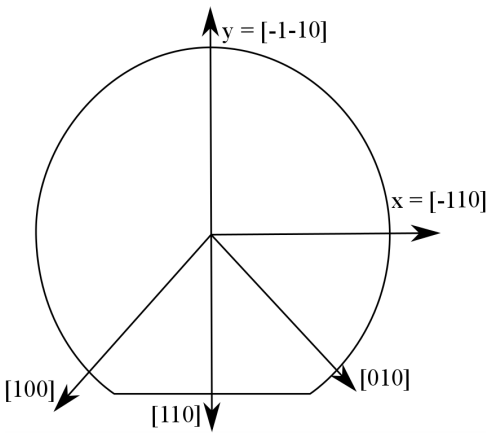


Fig. 1. Coordinate system for (100) Silicon.

V_{TH} - threshold voltage of MOSFET transistor;
μ - mobility of electrical carriers in transistor channels;
C_{ox} - capacitance of the oxide layer;
W - width of the MOSFET channel; and
L - length of the MOSFET channel.

It has been proven that the threshold voltage is independent of mechanical stresses [1]. Thus, a small change in the drain current induced by mechanical stresses mainly depends on mobility changes.

This can be described as [1]:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\mu}{\mu} \quad (4)$$

Mobility of electrical carriers is directly related to the resistivity of silicon [6]. Thus, the relationship can be written as:

$$\frac{\Delta\rho}{\rho} = -\frac{\Delta\mu}{\mu} \quad (5)$$

Combining 4 and 5 yields:

$$\frac{\Delta I_D}{I_D} = -\frac{\Delta\rho}{\rho} \quad (6)$$

The measured current values can be expressed in an incremental form as:

$$I_D = I_{D0} + \Delta I_D = I_{D0}\left(1 - \frac{\Delta\rho}{\rho}\right) \quad (7)$$

where I_{D0} is the reference current measured in the absence of mechanical stresses. Substituting Eqs. 1,2 into 7 yields [1]:

$$\frac{I_D\big|_{0^\circ} - I_D\big|_{90^\circ}}{I_D\big|_{0^\circ} + I_D\big|_{90^\circ}} = \frac{1}{2}\frac{-\pi_{44}^p(\sigma_{11}-\sigma_{22})}{1 - \pi_S^p\left(\frac{\sigma_{11}+\sigma_{22}}{2}\right) - \pi_{12}^p\sigma_{33} + f(\Delta T)} \quad (8)$$

$$\frac{I_D\big|_{+45^\circ} - I_D\big|_{-45^\circ}}{I_D\big|_{+45^\circ} + I_D\big|_{-45^\circ}} = \frac{-\pi_D^n\sigma_{12}}{1 - \pi_S^n\left(\frac{\sigma_{11}+\sigma_{22}}{2}\right) - \pi_{12}^n\sigma_{33} + f(\Delta T)} \quad (9)$$

where Π is the effective piezoresistive constants that is influenced by a circuit.

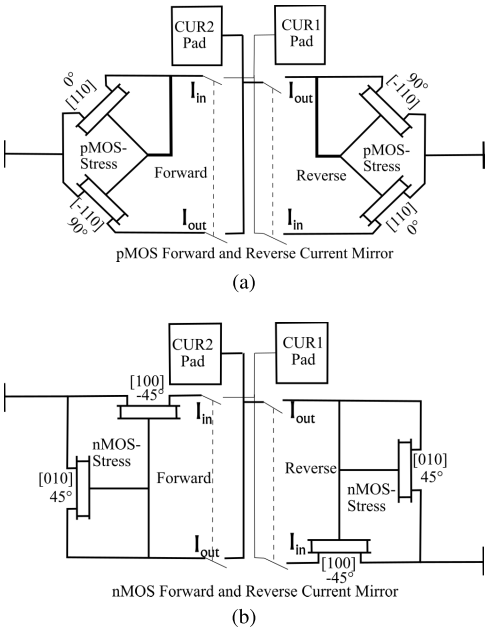


Fig. 2. Current mirror circuit used for stress measurement (a) pMOS current mirror used for measurement of the difference in normal in-plane stresses and (b) nMOS current mirror used for the in-plane shear stress measurement.

The normal stress difference, $D(\sigma) = \sigma_{11} - \sigma_{22}$, and the in-plane shear stress, σ_{12}, then, can be expressed as:

$$\sigma_{11} - \sigma_{22} = D(\sigma) = -\frac{2}{\pi_{44}^{p}(T)} \times \left(1 - \pi_S^p \left(\frac{\sigma_{11} + \sigma_{22}}{2}\right) - \pi_{12}^p \sigma_{33}\right) \left(\frac{I_D\Big|_{0^\circ} - I_D\Big|_{90^\circ}}{I_D\Big|_{0^\circ} + I_D\Big|_{90^\circ}}\right) \quad (10)$$

$$\sigma_{12} = \frac{-1}{\pi_D^n(T)} \times \left(1 - \pi_S^n \left(\frac{\sigma_{11} + \sigma_{22}}{2}\right) - \pi_{12}^n \sigma_{33}\right) \left(\frac{I_D\Big|_{+45^\circ} - I_D\Big|_{-45^\circ}}{I_D\Big|_{+45^\circ} + I_D\Big|_{-45^\circ}}\right) \quad (11)$$

It is important to note that the temperature term, $f(\Delta T)$, can be incorporated into the above governing equations by introducing the temperature-dependent piezoresistive coefficients, $\pi_{44}^p(T)$ and $\pi_D^n(T)$.

It is often assumed that the contributions of the sum of in-plane normal stresses, $\sigma_{11} + \sigma_{22}$, and the out-of-plane stress, σ_{33}, are negligible [1]; i.e.,

$$D^p = 1 - \pi_S^p \left(\frac{\sigma_{11} + \sigma_{22}}{2}\right) - \pi_{12}^p \sigma_{33} \approx 1 \quad (12)$$

$$D^n = 1 - \pi_S^n \left(\frac{\sigma_{11} + \sigma_{22}}{2}\right) - \pi_{12}^n \sigma_{33} \approx 1 \quad (13)$$

Then, Eqs. 8 and 9 can take the following forms [31]:

$$\sigma_{11} - \sigma_{22} = D(\sigma) \approx -\frac{2}{\pi_{44}^p(T)} \left(\frac{I_D\Big|_{0^\circ} - I_D\Big|_{90^\circ}}{I_D\Big|_{0^\circ} + I_D\Big|_{90^\circ}}\right) \quad (14)$$

$$\sigma_{12} \approx -\frac{1}{\pi_D^n(T)} \left(\frac{I_D\Big|_{+45^\circ} - I_D\Big|_{-45^\circ}}{I_D\Big|_{+45^\circ} + I_D\Big|_{-45^\circ}}\right) \quad (15)$$

In practice, current mirror circuits are utilized to measure the currents required in the above equations. Two current mirrors used in this study are shown in Figure 2, where a pair of MOS transistors is connected in each current mirror circuit. The branches of the current mirrors are oriented differently with respect to the crystallographic axes of silicon, which makes the transistors respond differently to applied mechanical stresses. The pMOS current mirror used for the normal stress difference measurement (Eq. 14) is shown in (a), and the nMOS current mirror used for the shear stress measurement (Eq. 15) is shown in (b).

The current mirror configuration is forcing the same current in both branches of the circuit if the parameters of both transistors are identical. When mechanical stresses are applied, the circuit becomes out of balance, and this effect is quantified by measuring the current differences in two branches of the current mirror. The applied stresses are determined from the measured current differences.

It is important to note that the current mirror device is not symmetrical. The input branches of the forward current mirrors contain pMOS oriented at 0° and nMOS oriented at −45°. In the reverse current mirrors, however, the input branches contain pMOS oriented at 90° and nMOS oriented at 45°. The effect of the inherently unsymmetrical configuration of current mirrors is canceled by averaging signals from the forward and reverse current mirrors.

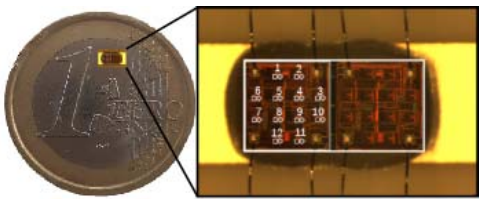
III. Sensor Chip and Data Acquisition

This section describes the sensor chip and the data acquisition unit used in the experiment.

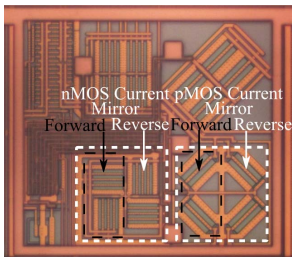
A. Sensor Chip Construction

The sensor chip consists of two sensors, as shown in Figure 3(a). Each sensor contains 12 measurement cells in a 4×4 matrix format. Four cells in the corners are inactive, and they are used as bonding pads.

The temperature-dependent piezoresistive coefficients, $\pi_{44}^p(T)$ and $\pi_D^n(T)$ were measured using an input current of 1 mA during device calibration. The same current was used for measurements to avoid a potential error associated with the current-dependent piezoresistive constants. First, the piezoresistive coefficient measurements are taken at room temperature (strictly laboratory temperature of 293°K) and then at different temperatures. The calibration is performed based on cutting parallel and diagonal stripes (30 pieces each) from the wafer. The parallel and diagonal direction is in agreement with the silicon independent piezoresistive coefficient direction. The 60 silicon stripes are distributed as randomly as possible over the wafer. Three wafers are considered in the calibration and the average value is used in the equation 16 and 17. It was found that the



(a)



(b)

Fig. 3. (a) Sensor chip containing two sensors where the numbers indicate 12 active measurement cells in each chip along with 1 euro coin size comparison; and (b) single measurement cell containing two current mirrors in a forward and reverse arrangement.

coefficients have a linear relationship with temperature as [31]:

$$\pi_{44}^{p}(T) = \beta_{44}^{p} \cdot (T - 293) + \pi_{44}^{p}(293) = -1.33 \cdot 10^{-3} \cdot (T - 293) + 1.008 \quad (16)$$

$$\pi_{D}^{n}(T) = \beta_{D}^{n} \cdot (T - 293) + \pi_{D}^{n}(293) = 0.83 \cdot 10^{-3} \cdot (T - 293) + 0.78 \quad (17)$$

where β is the fitted parameter and the unit of the coefficients is K/GPa. As shown in Figure 3 (b), each cell contains two pairs of stress sensitive pMOS and nMOS transistors. The channels of current mirrors are selected to produce the largest sensitivity to stresses. Each pair represents the forward and reverse current mirrors.

B. Data Acquisition Unit

The data from the sensors was collected by a dedicated acquisition unit. Control over the whole process was taken by a microcontroller. All inputs of the sensors were controlled by a digital-to-analog converter (DAC). It includes a voltage generator, which supplies power to the chip as well as the current source. Both of them were designed to ensure good stability and accuracy.

Outputs from the chip were digitalized by an analog-to-digital converter (ADC). The resolution of current measurement was approximately 0.0625 μA, and the total error of conversion was below 2 Least Significant Bit (LSB) [32]. The acquisition unit was able to measure eight sensors simultaneously, and the collected data was saved in a USB flash drive. It is noted that the data was saved in an unprocessed way, which means that only the measured values of currents and voltages are saved.

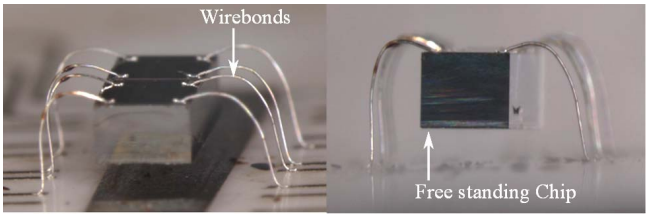


Fig. 4. Free-standing chip electrical connections.

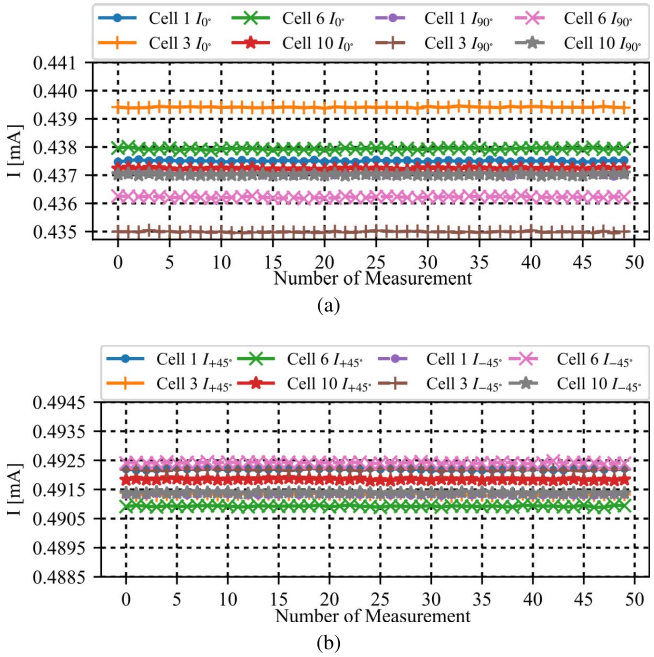


Fig. 5. Representative current values obtained at room temperature: (a) the average of $I_{0°}$ and $I_{+90°}$ of the pMOS current mirror and (b) the average of $I_{-45°}$ and $I_{+45°}$ of the nMOS current mirror.

IV. Uncertainty of Sensor Signal

Free-standing sensor chips are prepared to investigate the uncertainty of sensor signals. The random noise of the measurement system is evaluated first from signals obtained at room temperature. Then, the free-standing sensor chips are subjected to a thermal cycle, and the systematic noise associated with the temperature is evaluated.

A. Random Measurement Uncertainties

The following procedure was used to fabricate a free-standing sensor chip shown in Figure 4; (1) a sensor chip was first mounted on a low temperature co-fired ceramics (LTCC) substrate with a high temperature curing non-conductive adhesive; (2) the sensor pads and the LTCC pads were connected by wire bonds; and (3) the chip was unglued from the LTCC surface by dissolving the glue using a solvent. The free-standing chip was, thus, free from the CTE substrate effect.

Initial measurements were made at room temperature (20°C). The ADC had a sampling rate of 52,000 Samples per Second (SPS). During the Acquisition Unit (AU) development, a supplementary study was performed to examine how many samples would be required for a stable signal. The current

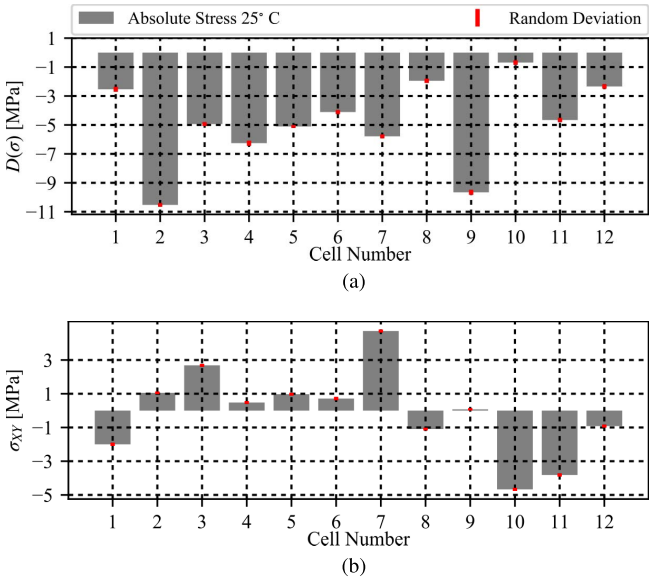


Fig. 6. (a) Normal stress difference and (b) shear stress obtained from a free standing chip at room temperature.

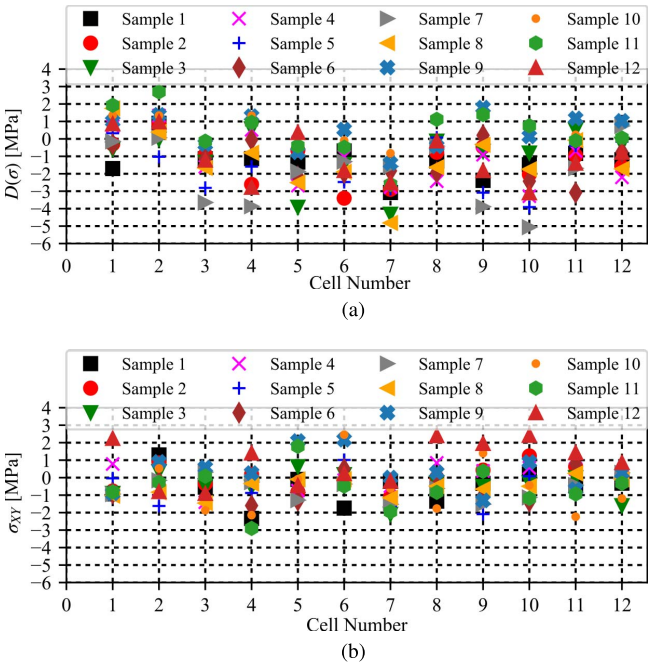


Fig. 7. (a) Normal stress difference and (b) shear stress obtained from 12 free standing chip at room temperature.

and voltage values of each phase were measured 40 times and were averaged. The whole cycle of sensor phase, cell and sensor switching takes around 2 minutes.

The representative current values of four cells measured at room temperature are shown in Figure 5. They were obtained by averaging the current values of the forward and reverse modes. The average current of the pMOS current mirror (I_{0° and I_{+90°) and the average of the nMOS current mirror (I_{-45° and I_{+45°) are shown in (a) and (b), respectively. A total of 50 measurements were made. Stable signals with low level random noise were observed.

The effect of the random noise on the uncertainty in stress measurements was evaluated. Figure 6 shows the normal stress difference and the shear stress of each cell measured from a free standing sensor chip at room temperature, where the error bars indicate the random noise determined from 50 measurements. The results indicate that the effect of the random noise on the stress calculations was virtually negligible: the average random uncertainty is only 0.072 MPa (1.49%) and 0.044 MPa (2.28%) for the stress difference and the shear stress, respectively.

It is important to note that stress values are high in some cells, and their magnitudes vary significantly from cell to cell, although the chip is not subject to any external loading (free-standing). This is attributed to the residual stresses of the chip produced by the manufacturing process, and this will be discussed in more detail later.

B. Systematic Uncertainty Associated With Residual Stresses

As observed earlier, the stress values of free-standing chips at room temperature have significant cell-to-cell variations. These stresses are not associated with any intended loadings, and should be negated for stress measurement applications. These residual stresses recorded on the free-standing chips are affected by the manufacturing process including wire bonding and metallization.

The stresses obtained from all 12 free-standing chips are summarized in Figure 7, where the stress difference and the shear stress of each cell are shown in (a) and (b), respectively. The results show significant chip-to-chip variations as well. Consequently, it does not seem practical to use the absolute stress values for any quantitative analyses due to this uncertainty. Instead, it is recommended to use the changes of stresses between two loading states because this uncertainty is presents in both loading states. The following experiment was conducted to illustrate this concept.

The 12 free-standing chips were subjected to a thermal cycles of −40°C and 125°C, and the relative stress difference and the shear stress caused by the thermal excursion were determined by subtracting the values at −40°C from the values at 125°C. The results are shown in Figure 8, where the error bars show the chip-to-chip variations. The average uncertainty ranges from -4 to 2 MPa over 12 cells. These values represent the effect of residual stresses on each cell caused by cooling the free-standing chips from 125°C to −40°C. The chip-to-chip variation is much smaller than that of the absolute stresses at room temperature (Figure 7). The manufacturing process should produce much larger in-plane normal stresses than in-plane shear stresses (σ_{XY}). It is expected that the manufacturing process would affect σ_{ZY} and σ_{ZX} more significantly. The values shown in Figure 8 can be used effectively to negate the systematic uncertainty associated with the residual stresses.

V. Accuracy of Load-Induced Stress Measurements

The accuracy of the sensor to measure the stresses produced by a thermo-mechanical loading is evaluated. A numerical

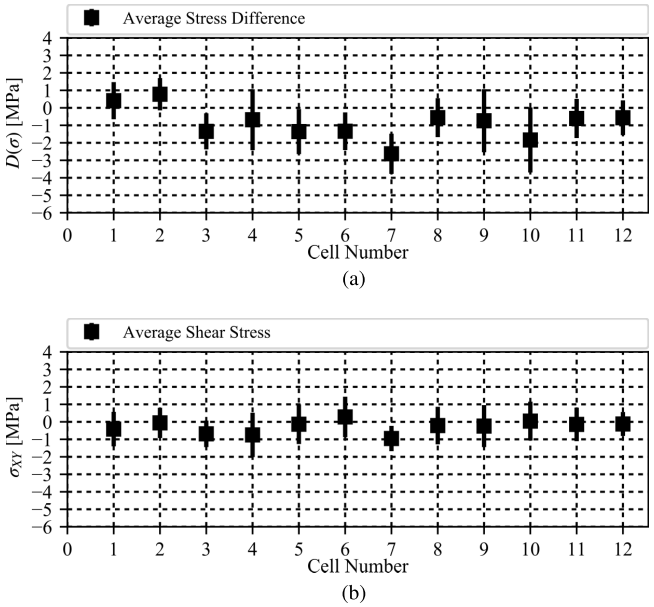


Fig. 8. Stresses of free standing chips, caused by cooling them from 125°C to −40°C: (a) the stress difference and (b) the shear stress.

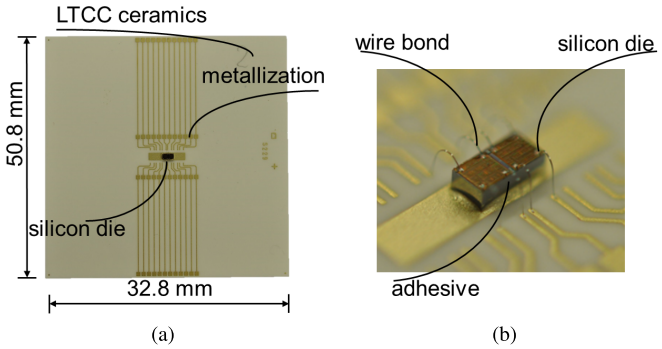


Fig. 9. LTCC Test Vehicle.

model is built and subsequently calibrated by an optical technique called moiré interferometry. The stresses of the cells predicted by the calibrated model are compared with the experimental data to establish the accuracy while taking the uncertainties discussed in Section IV into account.

A. Test Vehicle and Numerical Model Construction

A test vehicle used in the study is shown in Figure 9. The sensor chip was mounted on an LTCC substrate using a high temperature curing non-conductive adhesive. The electrical connection between the chips and the substrate was provided by a set of wire bonds.

B. Numerical Model Construction

The model construction started with preparation of the detailed geometry of the stress sensor. The geometrical model consisted of the significant details of the construction such as NiPdAu traces on the LTCC, detailed adhesive shape, and exact geometry of the chip. All these properties were obtained from the cross-sections using an optical microscope.

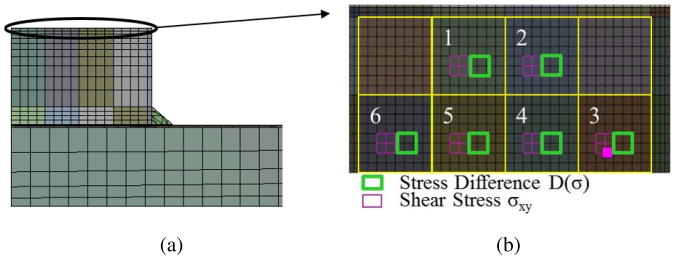


Fig. 10. Detailed mesh of the sensor chip: (a) side view and (b) top view where the elements used to extract stress are marked.

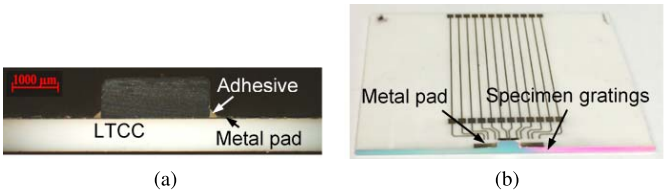


Fig. 11. (a) Specimen cross section (left); and (b) cross-section after replicating the specimen gratings.

A supplementary mesh sensitivity study was conducted, where mesh sizes were reduced until the stresses of the sensor remained constants. The element type was a higher order, 20 nodes hexahedral brick element with mid-side nodes. For the thin materials such as the die attach and the metal trace, a minimum of two elements were used through the thickness.

Another critical task of the modeling was to produce a detailed representation of the stress sensing cells. The thickness of the MOSFET branch in the actual sensor chip, in which the calculation of the stress was performed, was approximately 10 μm thick. The sensor chip was discretized to produce the 10 μm thick top layer, as shown in Figure 10(a).

In addition, each stress sensing cell was divided into 4x4 elements so that the elements matched to the geometry of current mirrors shown in Figure 3(b). The top view of the mesh is shown in Figure 10(b) to illustrate the mesh geometry more clearly. It shows the half of the sensor chip (half symmetry), where the elements corresponding the current mirrors for the normal stress difference and the shear stress calculations are marked by the green and purple squares, respectively.

The LTCC and the silicon die were modeled as isotropic elastic solid and orthotropic elastic solid, respectively. The properties of the die attach were measured by dynamic mechanical analyzer (DMA) and thermomechanical analyzer (TMA). It was also modeled as isotropic elastic solid with the temperature-dependent modulus of elasticity and coefficient of thermal expansion (CTE). Details of the material properties used in the numerical model are summarized in Table I. The glass transition temperature of the die attach was $100°C$. The total thickness of NiPdAu metal trace was 17 μm, while the thickness of Pd and Au was smaller than 1 μm. The effect of Pd and Au on the trace property was negligible, and the trace was modeled as pure Ni.

C. Model Validation by Moiré Interferometry

Moiré interferometry is a full-field optical technique to measure the in-plane deformations with high sensitivity, high

TABLE I
MATERIAL PROPERTIES

Material properties considered in the simulation	Modulus of elasticity $[MPa]$	CTE $[ppm/K]$	Material law
LTCC	128000	4.5	Linear-elastic
Silicon die	167000	2.8	Linear-elastic
Metallization	80000	17	Linear-elastic
Die attach	3940	40	Linear-elastic

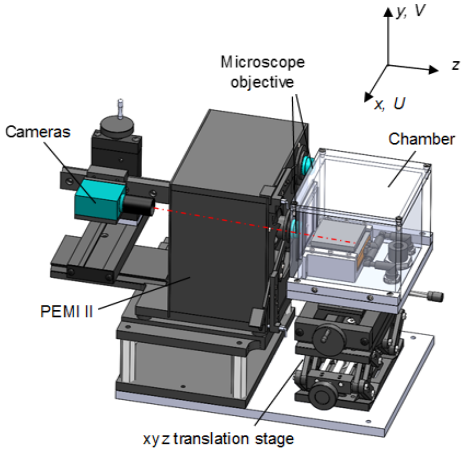
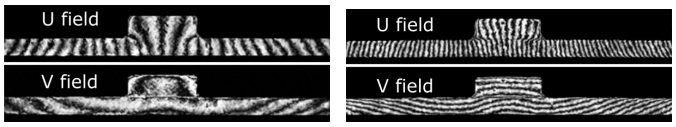


Fig. 12. Schematic illustration of the optical/mechanical configuration of an advanced portable moiré system.



(a) (b)

Fig. 13. Fringe patterns representing in-plane displacements obtained at (a) −40°C and (b) 125°C, where the contour interval is 104nm.

signal-to-noise ratio, and excellent clarity [33]. The outputs are the contour maps of in-plane displacements. It has been used widely for electronic packaging design and reliability assessment [34].

In this work, an advanced moiré interferometry system was used to document the required deformation fields. The system is illustrated in Figure 12. It consists of (1) a portable engineering moiré interferometer that provides two sets of virtual reference gratings, (2) a conduction chamber built on a high performance thermo-electric cooler that provides accurate temperature control, and (3) a high-resolution digital camera with a microscope objective lens. The thermal conduction chamber is mounted on an x-y-z translation stage, which allows positioning as well as focusing the specimen. More details of the system can be found in [35]. A virtual reference grating, f, was formed by two coherent beams of light provided by the interferometer. The deformed specimen grating and the uniform reference grating interacted to produce moiré patterns of in-plane displacements.

To obtain more detailed displacement fields around the chip, the measurement sensitivity was improved further by

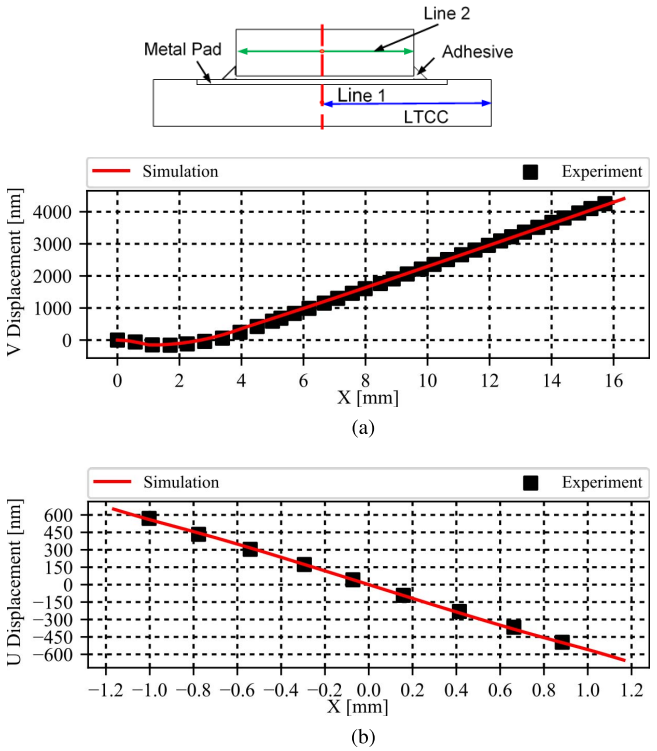


Fig. 14. Comparison of experimental data with numerical results: (a) the y-displacement along Line 1 and (b) the x-displacement along Line 2.

an image processing scheme called the optical/digital fringe multiplication method [33]. The final fringe patterns representing the thermally-induced displacements are shown in Figure 13, where the contour interval is 104 nm displacement per fringe order. The fringe patterns represent the relative displacement along the x (or U) and y (or V) directions, caused by heating (125°C) or cooling (−40°C) the assembly from the reference temperature (room).

Another detailed 3-D model whose dimensions were identical to the moiré specimens was constructed for model validation. A traction-free boundary condition was imposed on the cross sections to simulate the moiré experiments.

The displacements at 125°C and −40°C were extracted from the fringe patterns, and the deformations caused by cooling the assembly from 125°C to −40°C were compared with the modelling results. The results are shown in Figure 14, where the displacements along Lines 1 and 2 shown in the inset are compared with the numerical predictions. The data match to each other very well, which verifies the validity of the numerical model.

It is worth mentioning that the initial comparison was not as good as shown in Figure 14. Several adjustments were made to achieve the high level of validity. The most critical adjustment was: (1) the position of the metal trace and metal pad layer and (2) the LTCC thickness. In the initial attempt, they were modeled as a separate layer on the top of the LTCC substrate. It was found from a closer examination that they were embedded in the LTCC substrate, and the model was corrected accordingly. Also, the LTCC thickness was initially larger in comparison to the cross-section findings. The effect

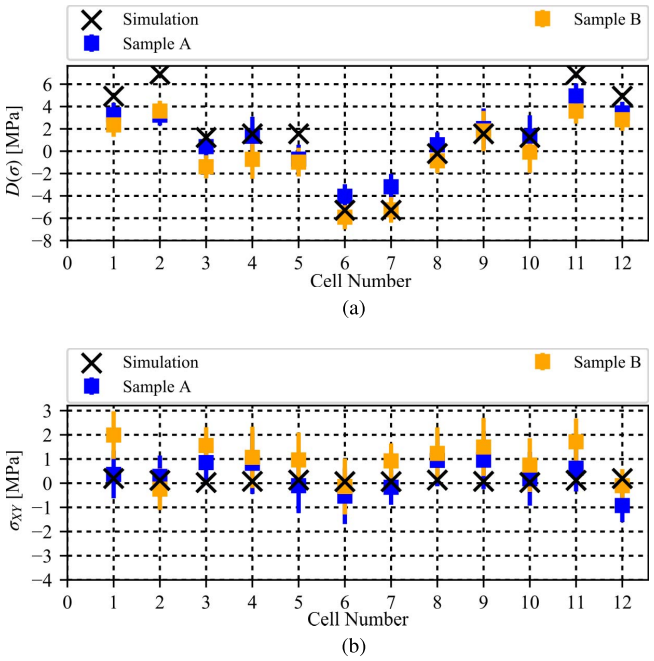


Fig. 15. Comparison of experimental data with numerical results: (a) the normal stress difference and (b) the shear stress.

of the LTCC thickness on the deformation was significant due to its high volume, and this adjustment brought the agreement to the desired level.

D. Accuracy of Load-Induced Stress Measurements

The predictive FEM model was used to evaluate the accuracy of the sensor measurements under an in-situ loading condition. The stress at each stress sensing element group was evaluated using the stress averaged over the corresponding four elements.

Two LTCC assemblies (Figure 9) were subjected to the same thermal cycle used for the moiré experiment. The stress signals were obtained at the peak temperatures (125°C and −40°C). The normal stress difference and the shear stresses at −40°C were then subtracted from those at 125°C.

The normal stress difference and the shear stress predicted by the model are compared with experimental data in Figure 15. It is important to note that the systematic uncertainty determined from the free-standing sensors were subtracted from the experimental data. The error bars indicate the standard deviations of the systematic uncertainties.

The stress difference shows good agreement not only in the trend but also in the magnitudes within the systematic uncertainty. This level of agreement is excellent for stress comparison, which is typically a lot more challenging than displacement or strain comparisons. The magnitude of the shear stress, however, is much smaller than the systematic uncertainty. The in-plane shear stress may not be useful for typical electronics packaging applications.

VI. Conclusion

The random and systematic measurement uncertainties of the CMOS-based piezoresistive stress sensor were evaluated. The random uncertainty associated with the data acquisition unit was evaluated first using the raw current data obtained from uniquely fabricated free-standing sensor chips. The results obtained from 50 repetitions indicated that the random uncertainty was negligible. The stress measurements of the free-standing sensor chips proceeded to evaluate the systematic uncertainties associated with the manufacturing-induced residual stresses. The stresses obtained from the free-standing sensor chips indicated significant cell-to-cell as well as chip-to-chip variations. It was recommended that only the changes between two loading states be used for actual applications. A procedure to negate the systematic uncertainties was also proposed and implemented. Finally, the stress measurement accuracy of the sensor chip under an in-situ loading was quantified by a numerical model verified by a sub-micron sensitivity optical technique called moiré interferometry. When the systematic uncertainty determined from the free-standing sensor chips were subtracted from the experimental data, the normal stress difference showed excellent agreement with the numerical prediction. However, the magnitudes of the shear stresses were so low that the systematic uncertainties dominated the shear stress signals. It was also recommended that only the normal stress difference be used for actual applications.

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