Pentium Pro Architecture Overview

Presented by

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“New” To the 80x86 world

- Decoupled Architecture
- Superpipeline (12 stages)
- Glueless SMP
- Out of Order (Speculative) Execution
- Dual inline Bus (Marketing term)
- Misc. (BIST, Performance counters . . .)

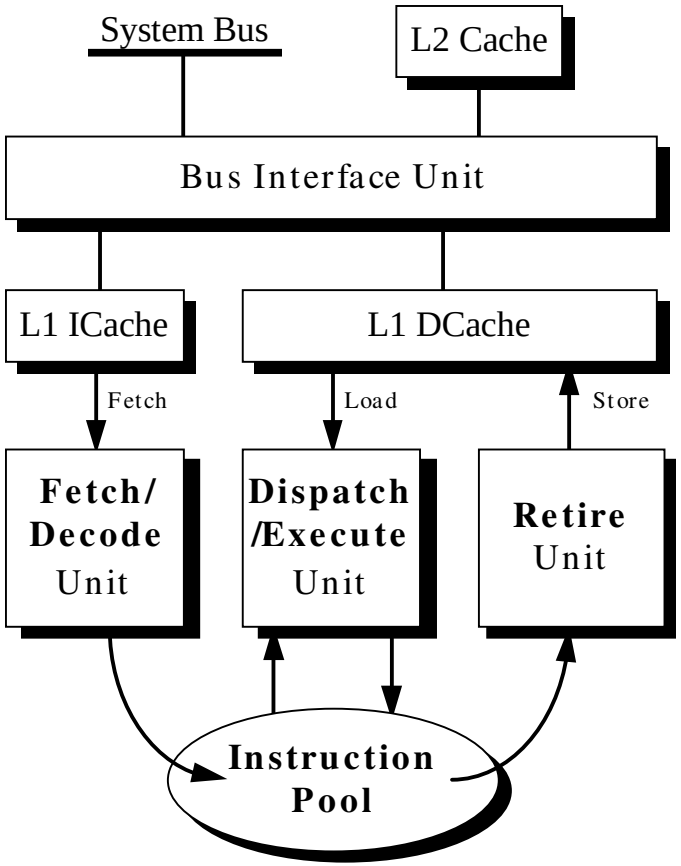
Design Goals

- 2X faster than Pentium on same process technology
- Total x86 compatibility
- “looks and feels” like a fast 80486.

Basic Ideas

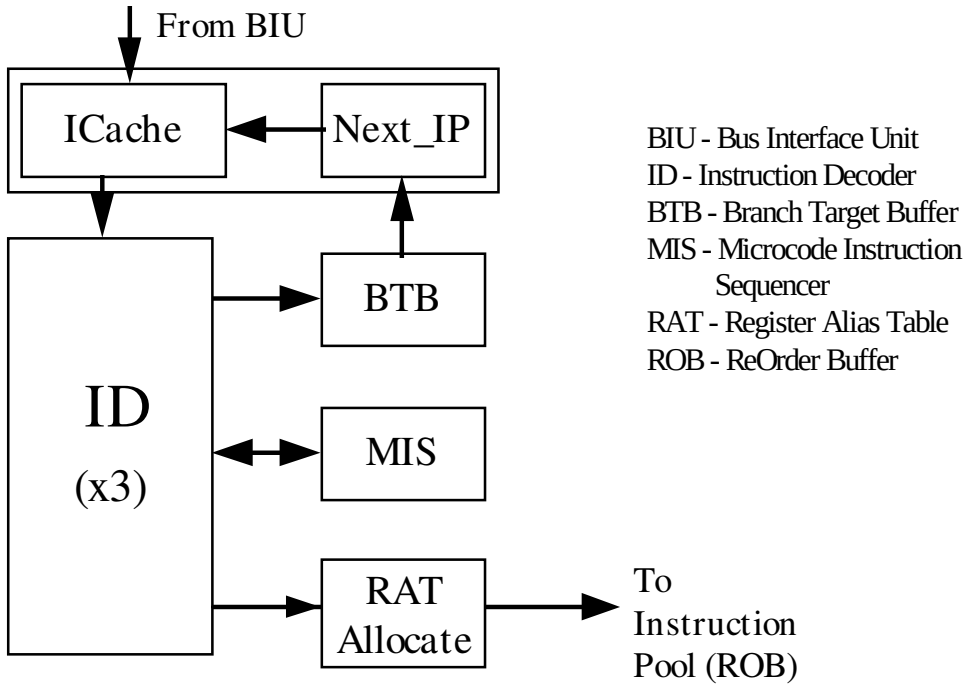
- x86 instructions decoded into uops.
- uops are simple, risc-ish instructions
- maximum of 3 uops maybe issued per cycle.
- maximum of 3 uops maybe retired per cycle.
- Maximum of 5 uops maybe executing OOO per cycle.(resource availability/dependency)

Block Diagram

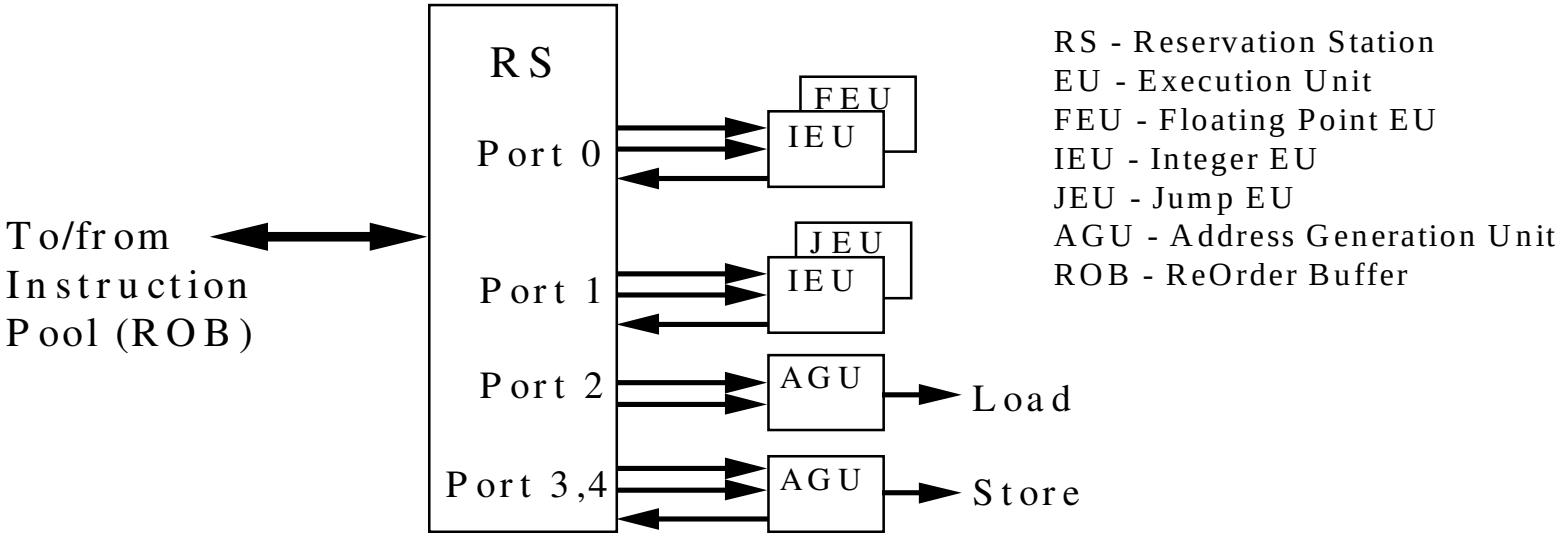


Fetch/Decode Unit

- decode maximum of 3 variable length instructions per cycle
- brute force decoding on byte boundaries, toss invalid results
- 2 “simple” decoders and 1 MIS
- Patchable Microcode
- fetches past unresolved branches based on prediction
- large register file for register renaming.

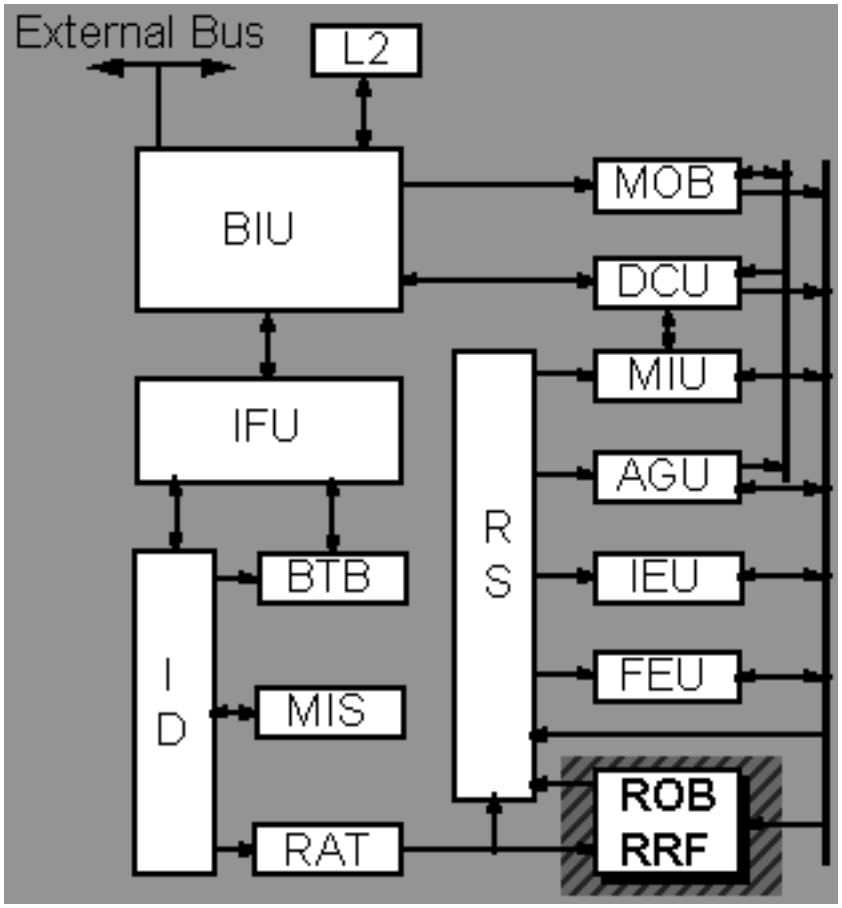


OOO Execution



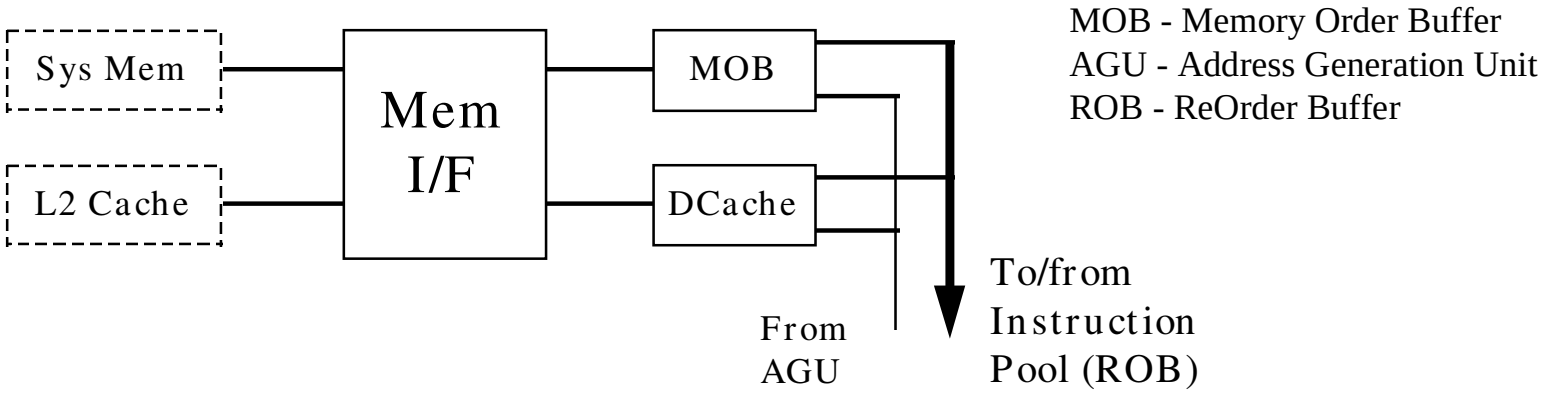
- Instructions executed OOO, when operands are ready, and resources are available.
- Instructions past unresolved branches are also executed speculatively.

Retirement



- uops recombined at ROB
- results commited to “machine state” in program order.
- x86 compatibility ensured.

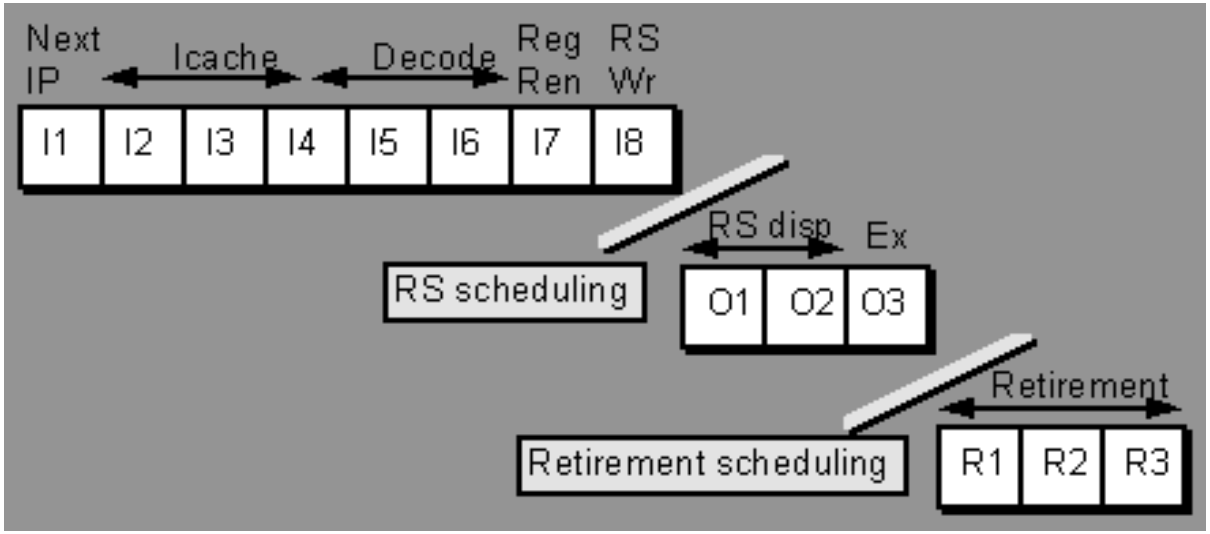
Bus Interface Unit



- Loads may bypass stores.
- Loads may bypass loads.
- Stores may not bypass loads.
- requests issued to L1 and L2 simultaneously, L2 request squashed if data is present in L1.

Decoupled Architecture

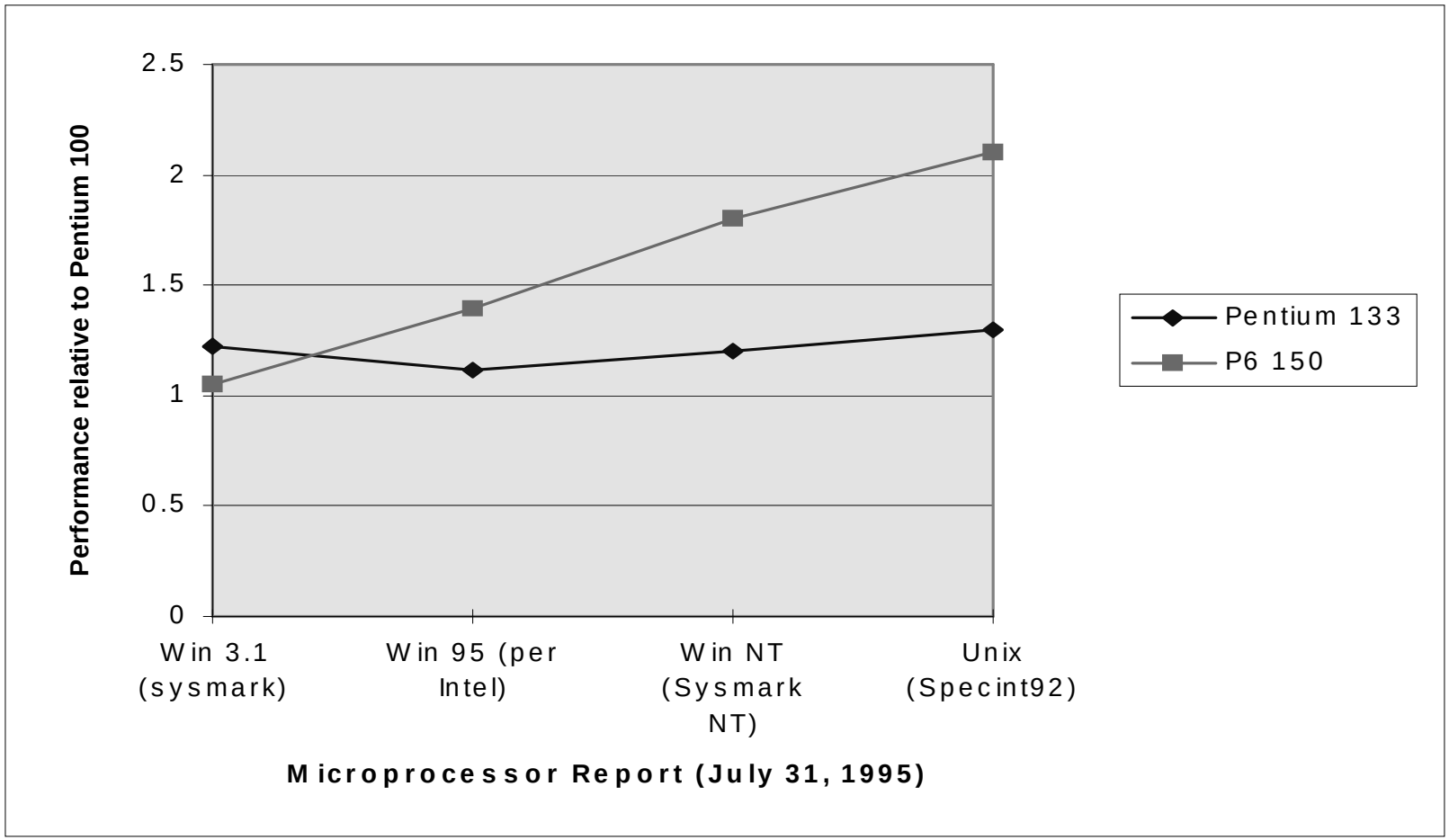
- ISA no longer implied microarchitectural implementation.
- “execution” occurs before commitment to state.



P6 Glass Jaw issues (16 bit code)

- Branch Misprediction.
- Partial Register usage (al, ah, ax, eax)
- Segment register
- Unaligned data access
- Compiled code excels.
- Legacy hand assembly code suffers.

Performance relative to Pentium 100



Glueless SMP

- MESI protocol
- GTL+ bus
- Integrated L2 reduces memory bus contention.
- Up to 4 processors per cluster.

Pentium II GTL+ Bus

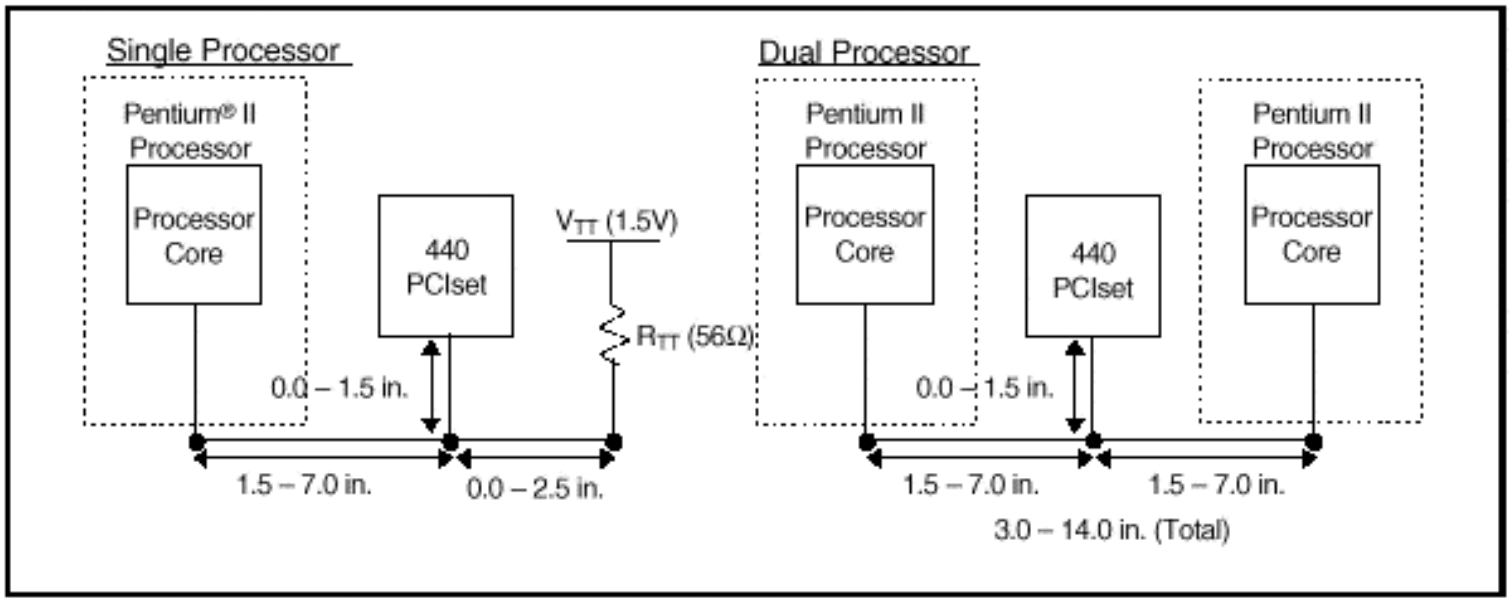


Figure 2. Pentium® II Processor General GTL+ Interconnect and Topology Guidelines

Other Features

- BIST
- Built in performance counters
- Patchable microcode
- ECC protected L2 cache

Pentium Pro and Pentium II differences

- Outsourced L2 cache.
- L1 doubled to 16K/16K
- Segment registers cached
- MMX bolted on

Future Developments

- Intel now split between IA-32 and IA-64
- More IA-32 still being designed
- Deschute: 0.25um process shrink
- ???? (Hint: Read Microprocessor Report)
- MMX2?

Conclusion

- P6 is a Brainiac CPU
- Decouples ISA from microarchitectural implementation
- Basis for future IA-32 processors
- importance of workload selection