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Memory Systems

Spring 2014

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Lecture B

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David Wang
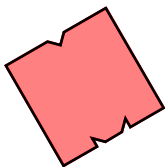
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SLIDE 1

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# CS-590.26, Spring 2014

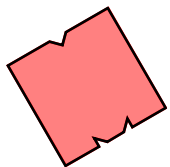# *High Speed Memory Systems: Architecture and Performance Analysis*
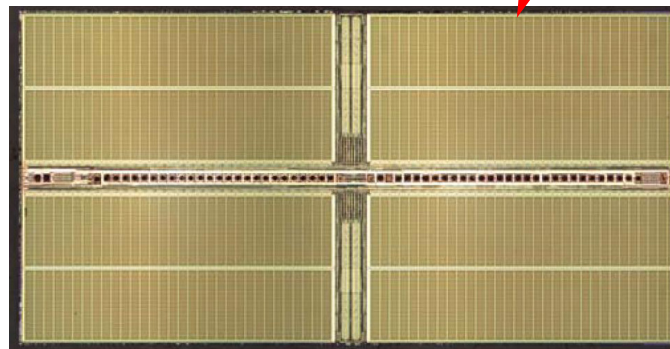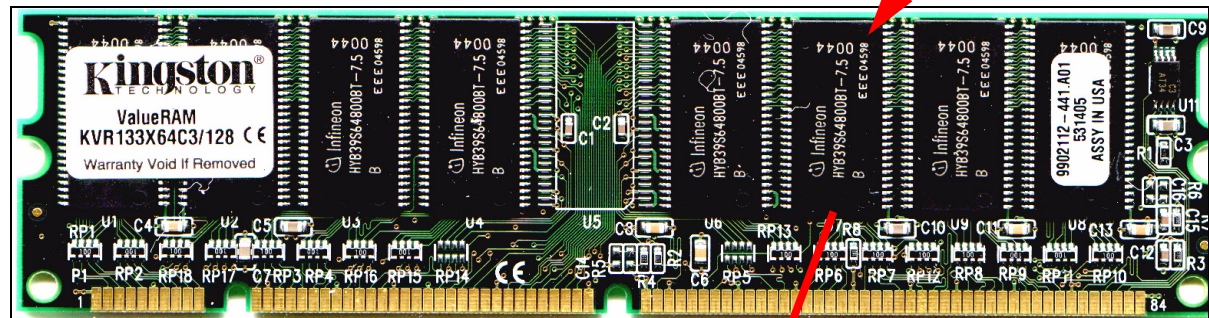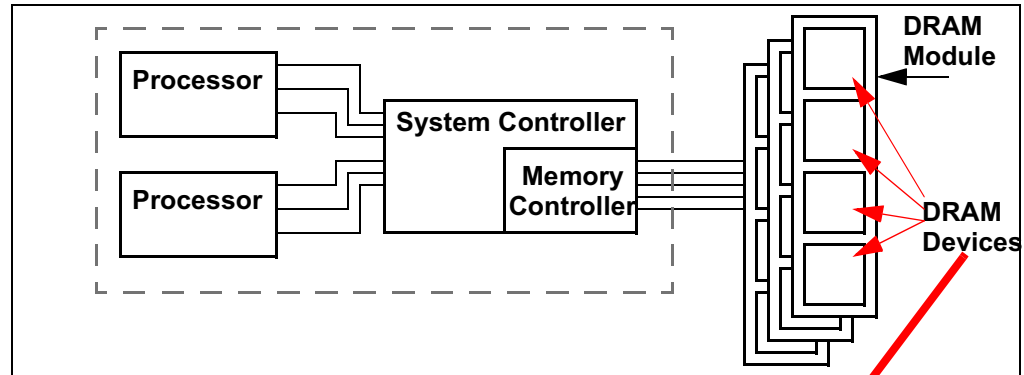
# *DRAM Device Circuits and Architecture*

**Credit where credit is due**:
Slides contain original artwork (© Jacob, Wang 2005)

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# Overview

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# DRAM Device Architecture



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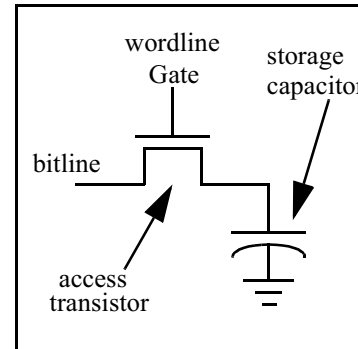Spring 2014

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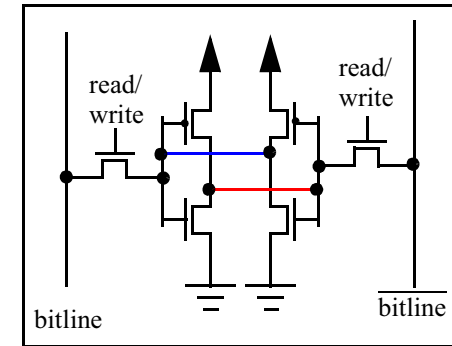of Crete

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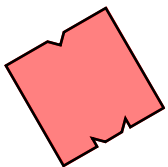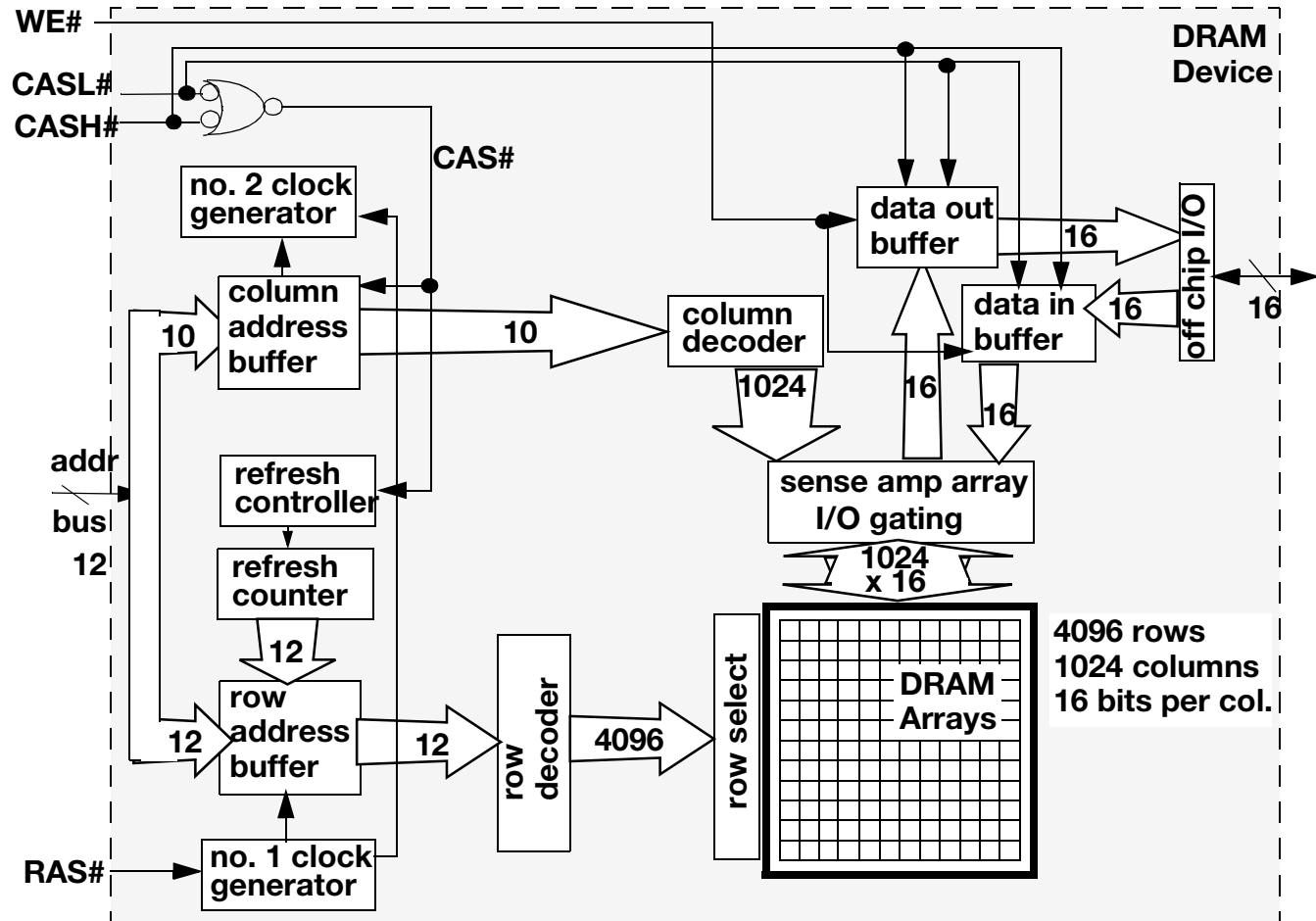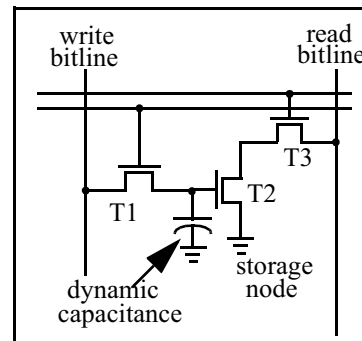
# Storage Cells



**3T1C
storage cell
(original DRAM)**

**1T1C
storage cell
(classic DRAM)**

**6T
storage cell
(classic SRAM)**

**DRAM: Dynamic Random Access Memory**

**How long does "memory storage" last?**

**Cell capacitance vs Leakage current**

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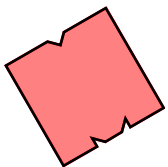
# Storage Cell Structure I

**plate capacitor**



**above
silicon in poly**
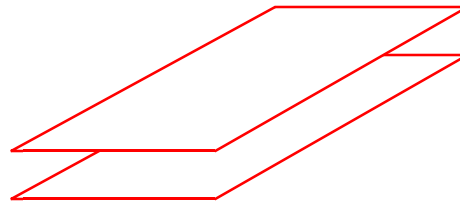
$$C = \varepsilon \frac{A}{d}$$

**Shrinking DRAM devices
means reduced cross
section (area)**
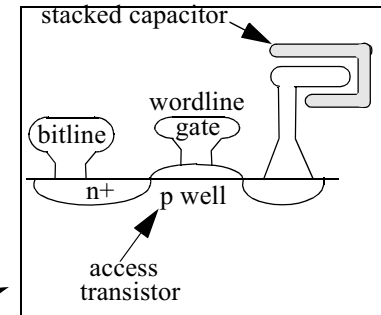


**below silicon
surface in trench**

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# Storage Cell Structure II



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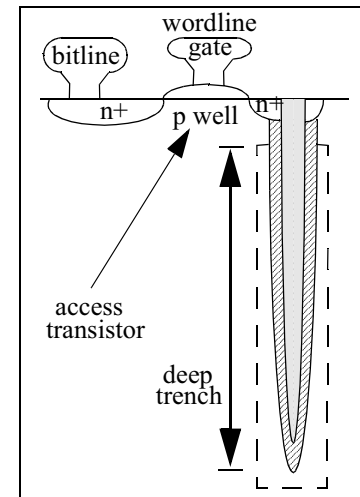Memory Systems

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# DRAM Array I

bitline
contact

storage
capacitor

unit
cell

wordline
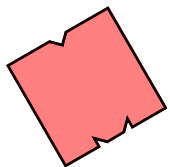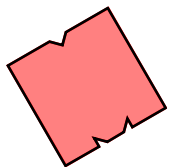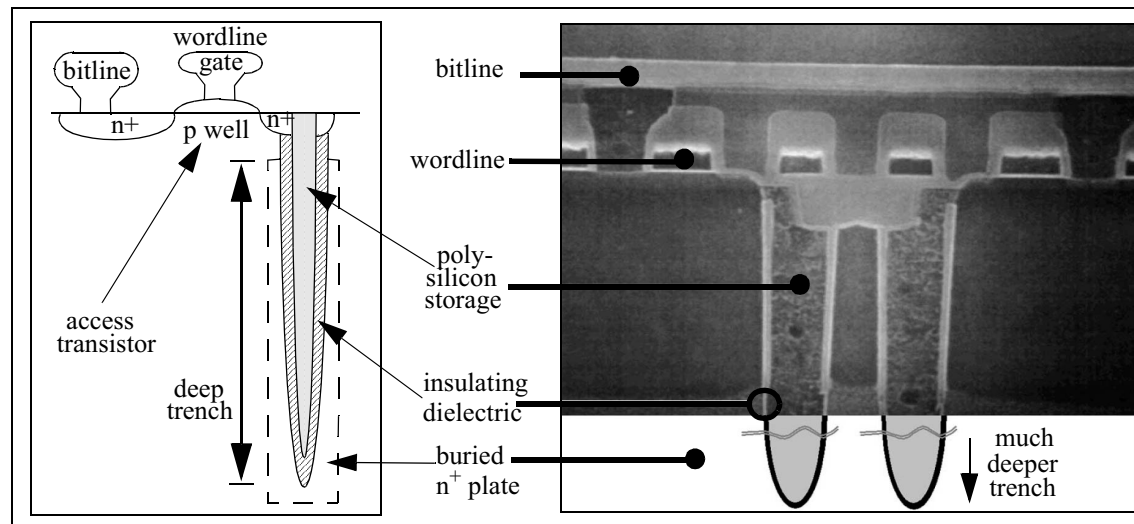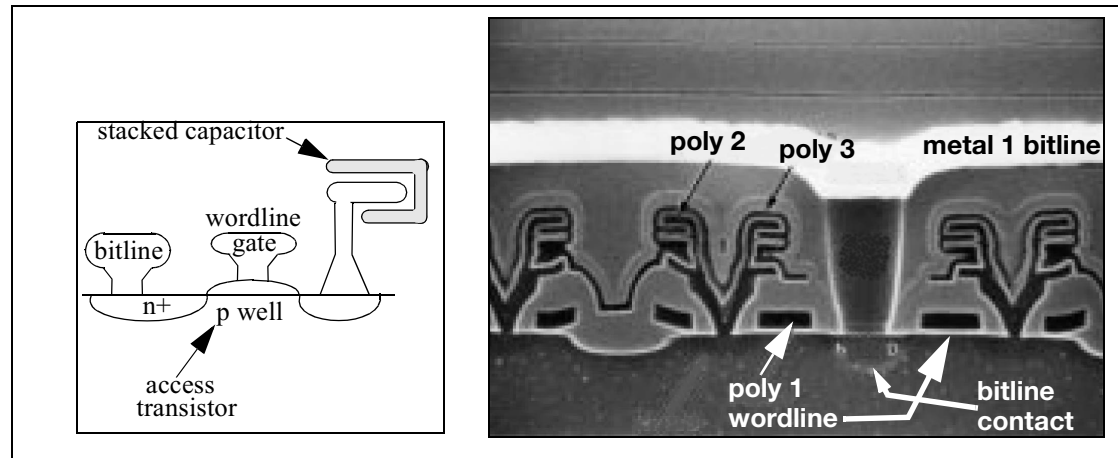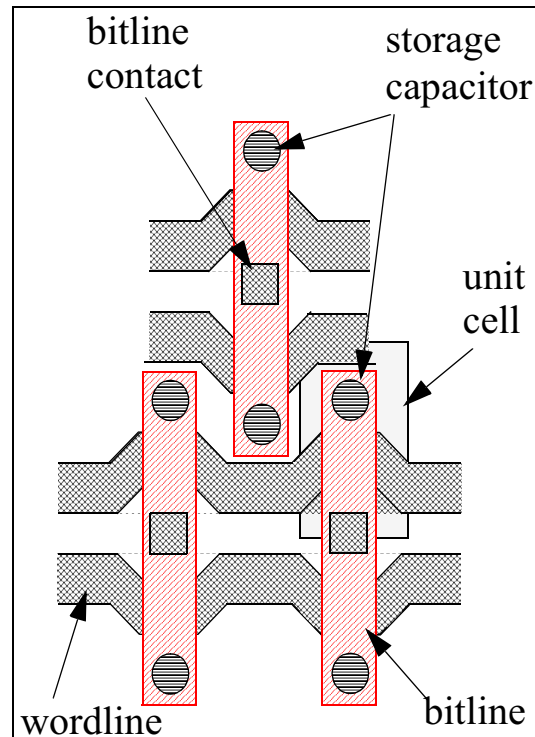
bitline

## 8F$^2$ cell

**(F = feature size. 90nm etc)**
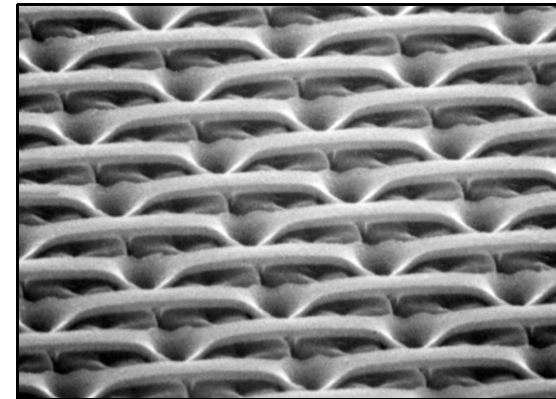


**Polycide Bitlines**
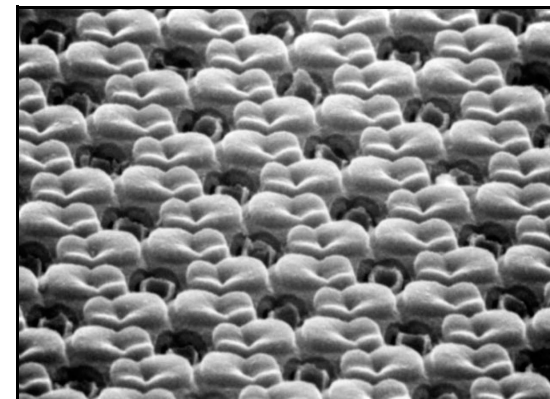


**Unlayered
DRAM Cell Array**

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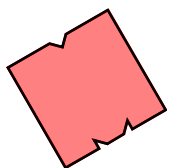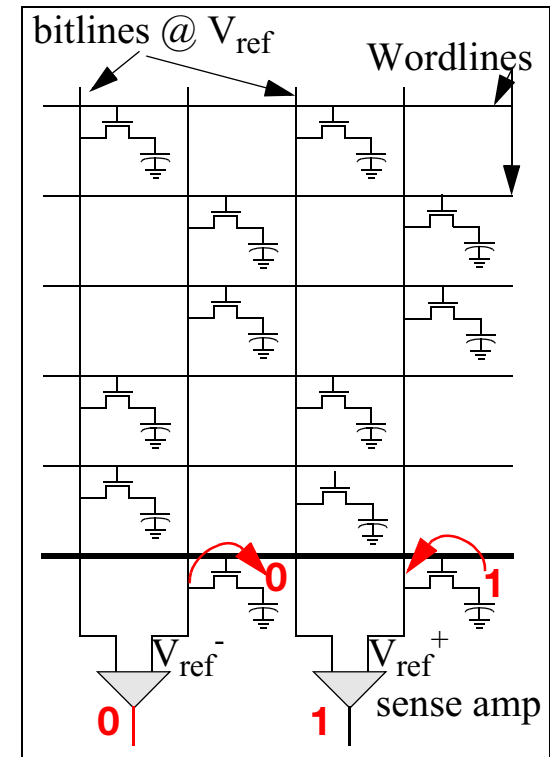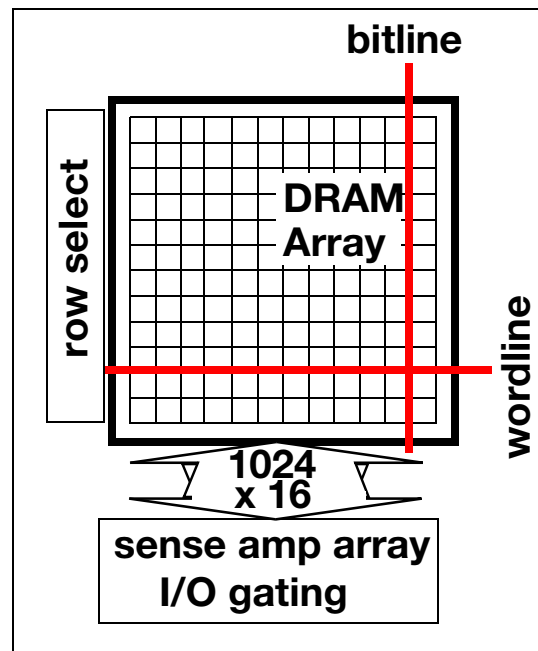
# DRAM Array II



**Note the direction of the arrows—storage via capacitance**

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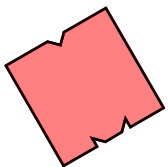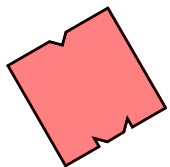
# DRAM Array III (folded bitline)
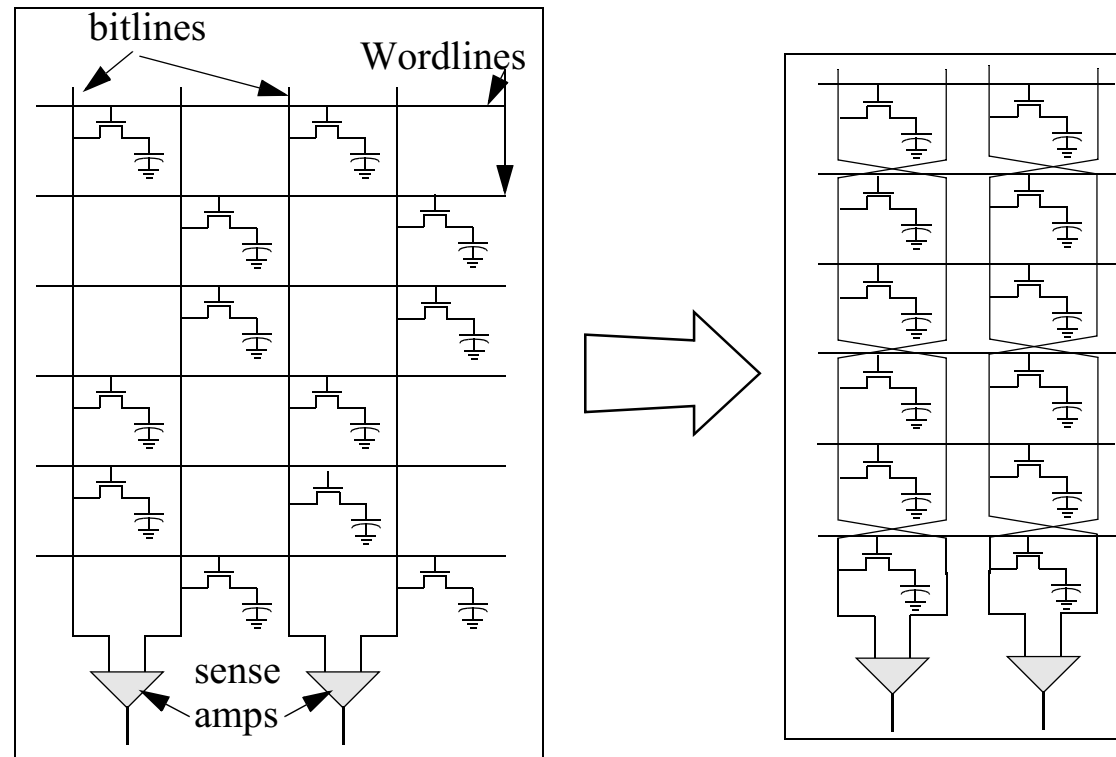


**2 Bitline lanes through each cell (larger cell size)**

**Cell size: typically 8 $F^2$**

**Better noise tolerance (common mode rejection)**

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# DRAM Array IV (Open Bitline)

bitlines    Wordlines
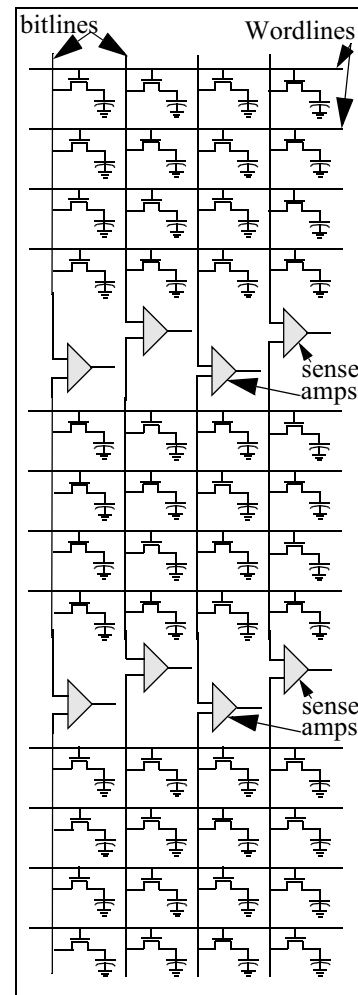
**Dummy structures
at array edges**

sense
amps

**1 Bitline lane through each cell**

**Cell size: typically 6 F$^2$**

sense
amps

**Bitline pairs comes from
different array segments**

**Challenge: How to get good noise tolerance
AND small cell size?**

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# Sense Amplifier



**Wordlines**

**voltage eq. circuit**

**sensing circuit**

**input write driver**

**Bitline**

$\overline{\text{Bitline}}$

**output**

$\overline{\text{input}}$
**write driver**

$\overline{\text{output}}$

$\frac{V_{cc}}{2}$

**input write driver**

**Bitline**

$\overline{\text{Bitline}}$

**output**

$\overline{\text{input}}$
**write driver**

$\overline{\text{output}}$

**SAN**  **SAP**  **EQ**  **CSL**  **WE**

**Differential**

**Control Signals**

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# Array Precharge

**Wordlines**

## Precharge

**1**  **1**

**sensing circuit**   **voltage eq. circuit**

**input write driver**

$V_{ref}$

**Bitline**

**output**

**0**  **1**

$\frac{v_{cc}}{2}$

**input write driver**

$V_{ref}$

**Bitline**

**output**

**SAN**   **SAP**   **EQ**   **CSL**   **WE**   **output**

## Assert equalize, Array precharged to $V_{ref}$ (typically $V_{cc}/2$)

**0**   $V_{ref}^{-}$   $V_{ref}$   $V_{ref}^{+}$   **1**

## Voltage color chart

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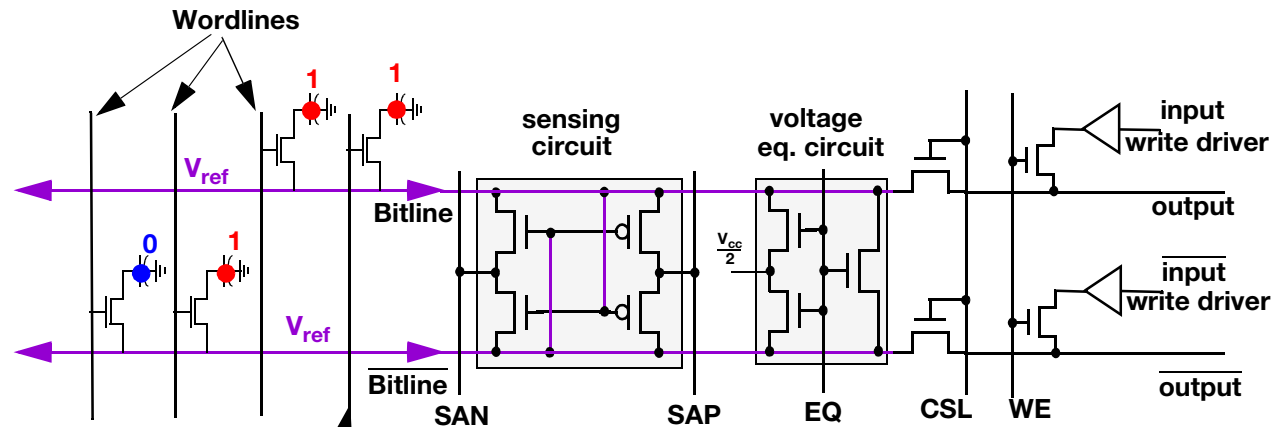
# Row Access 0



about to select this row (wordline)

timeline

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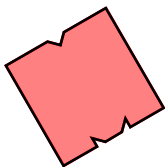
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# An Aside: the Sense Amp

**Bitline**

**Bitline**

**SAN**

**SAP**

**goes to GND**

**goes to Vcc**

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# An Aside: the Sense Amp

**Bitline**

**Bitline**

**SAN**

**goes to GND**

**SAP**

**goes to Vcc**

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# Row Access 0



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# Row Access I



**selected row (wordline) activated**

**timeline**

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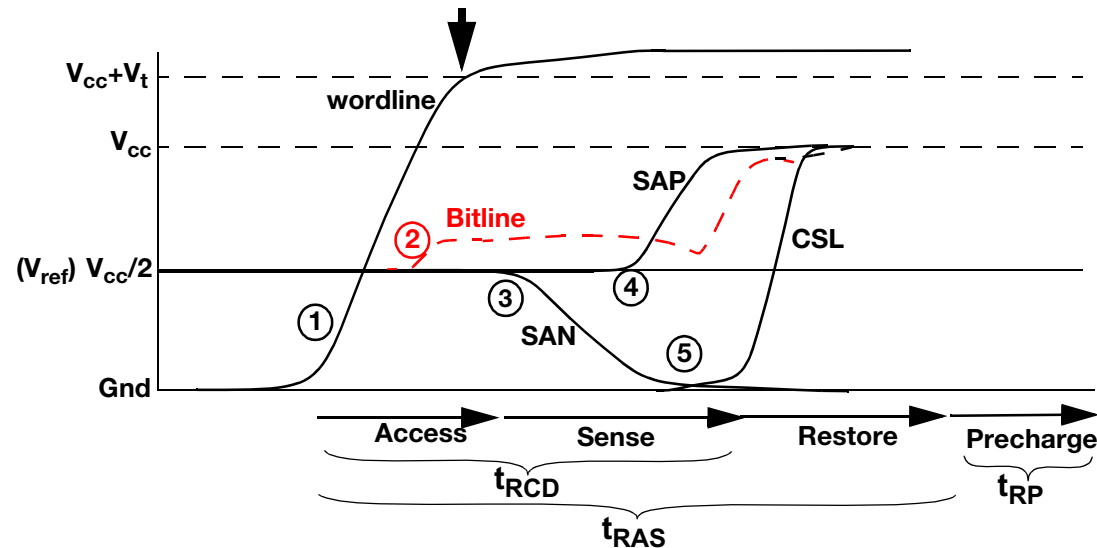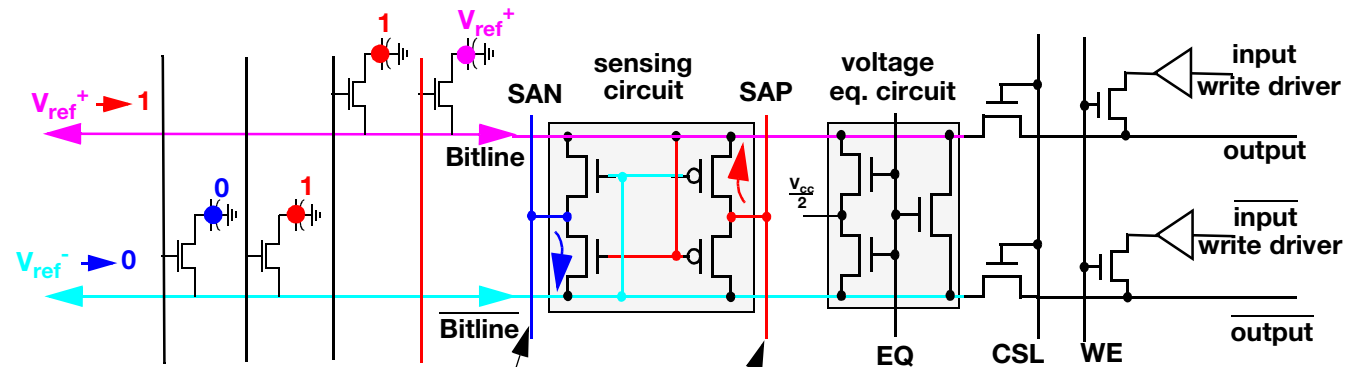
# Row Access II (sense)



**SAN and SAP control signals active
lower NFet more conductive, upper PFet more conductive.
Bitline pairs slammed to opposite voltage rails, then upper
NFet and lower PFet shut off completely.**

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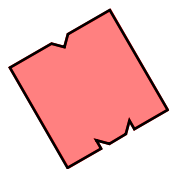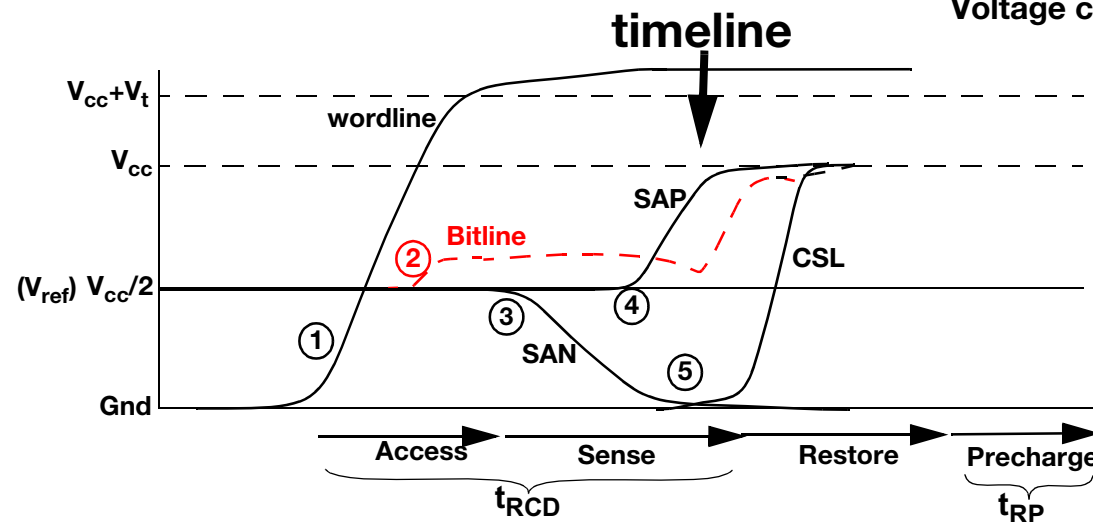
# Row Access III (Restore)
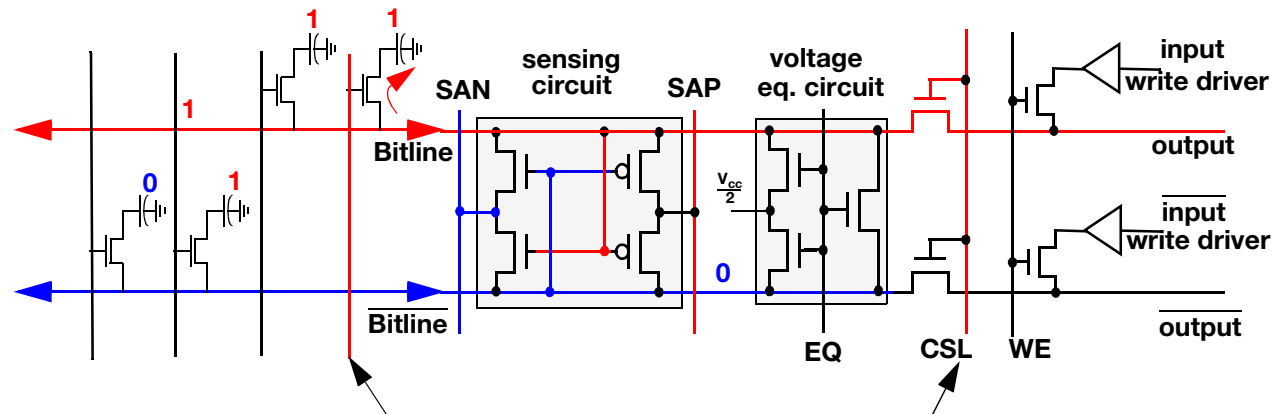


**Wordline kept open, now bitline potential drives the full voltage level "1" back into cell. If the column is selected, data is driven out to rest of the world.**

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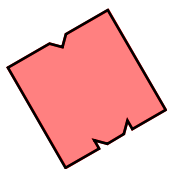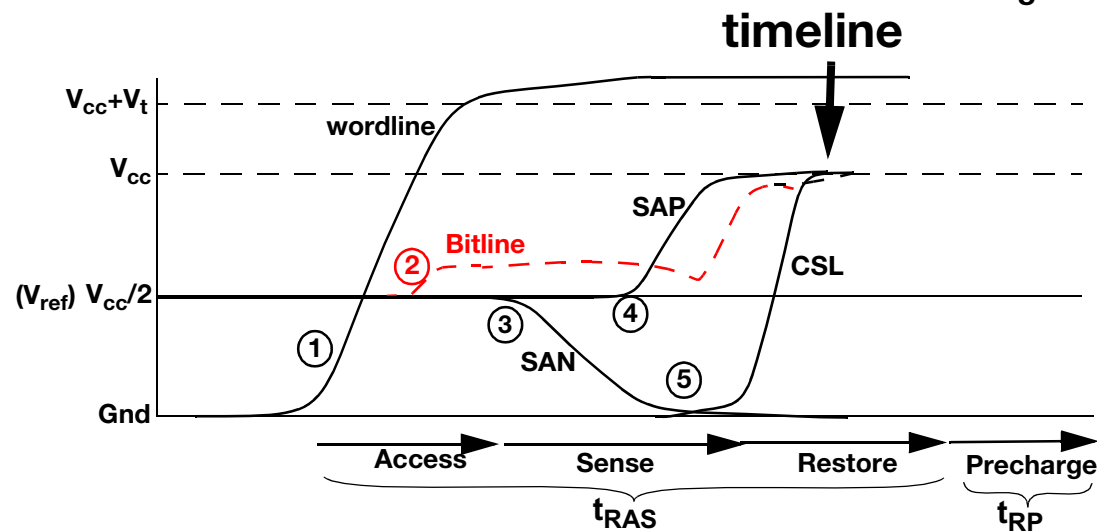
# Write (over old data)
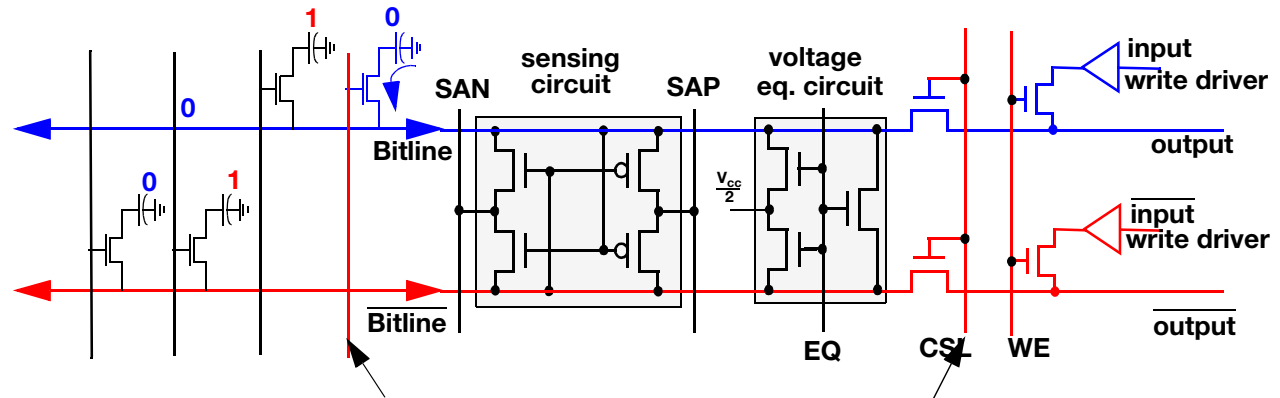


**Wordline is still open, input write driver drives the full voltage level "0" into cell.**

0   $V_{ref}^-$   $V_{ref}$   $V_{ref}^+$   1
**Voltage color chart**

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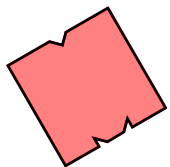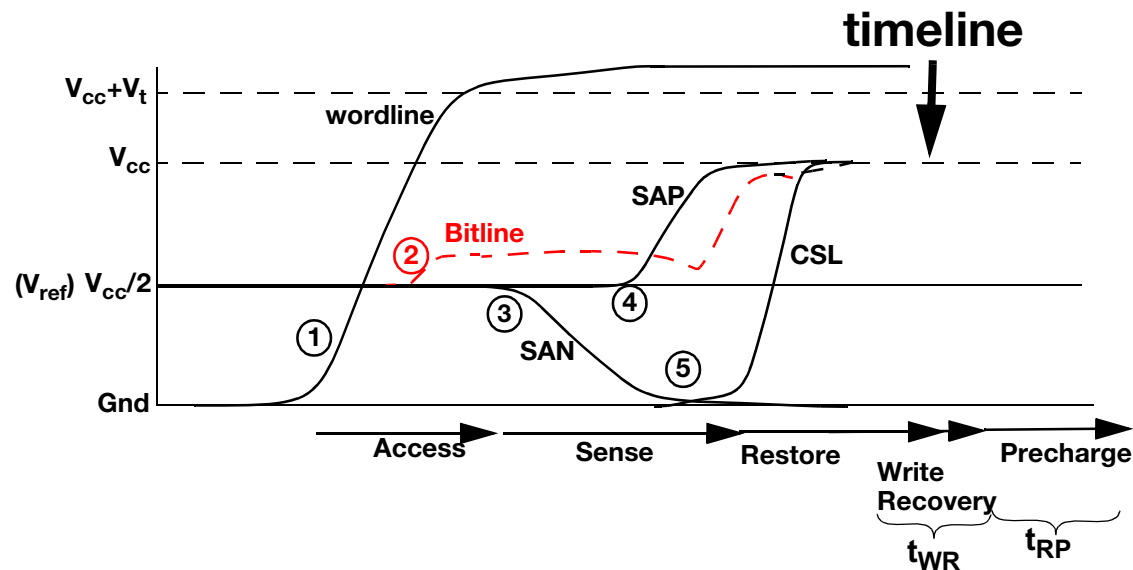
# Decoders and Redundancy



**defect (hard error)**

**spare columns (bitlines)**

**row decoder**
**n to $2^n$ + m decode**

$2^n$ **rows**

**column select**

**m spare rows (wordlines)**
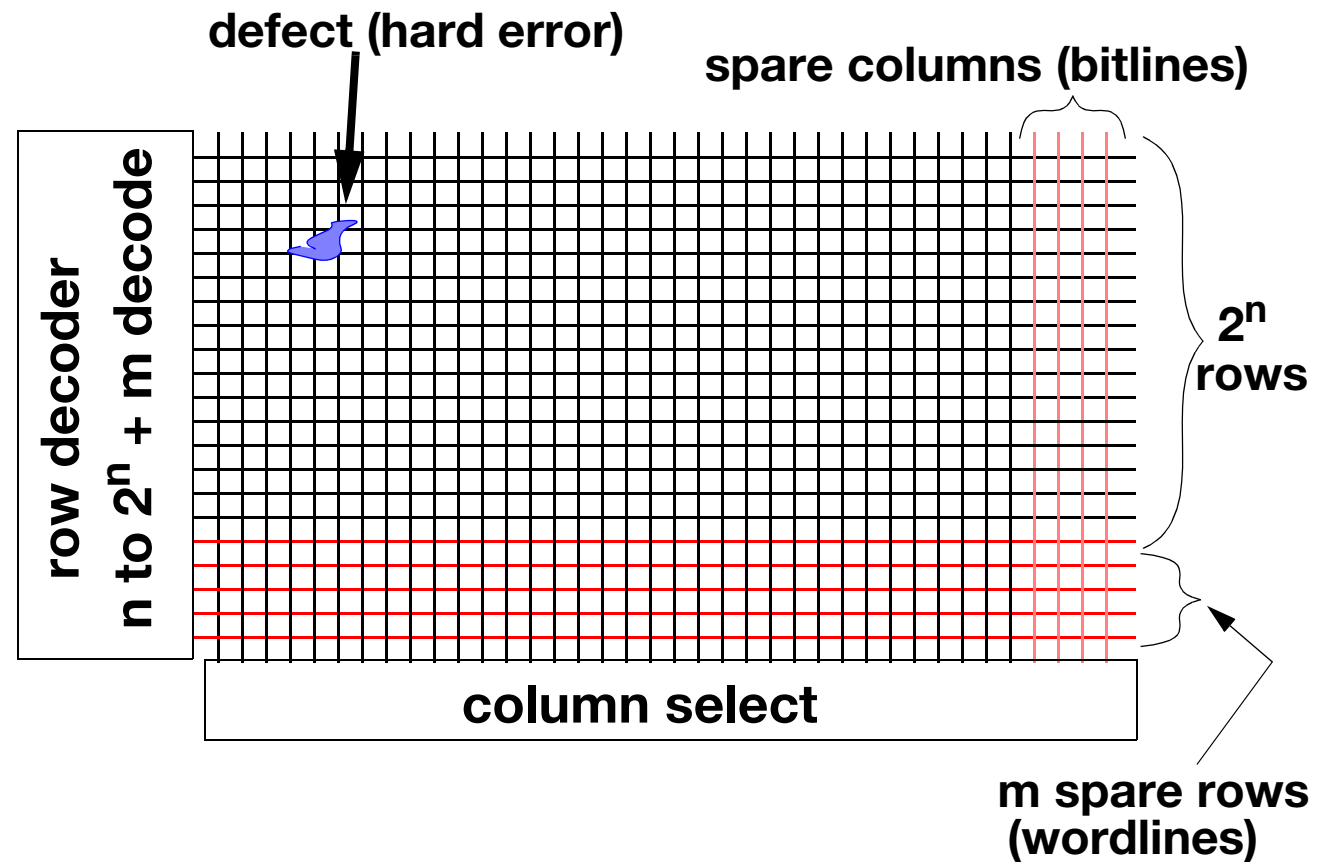
**Challenge: How to get good yield and tolerate *some* defect?**

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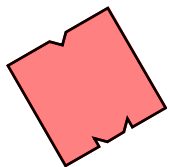
# Programmable Decoders I
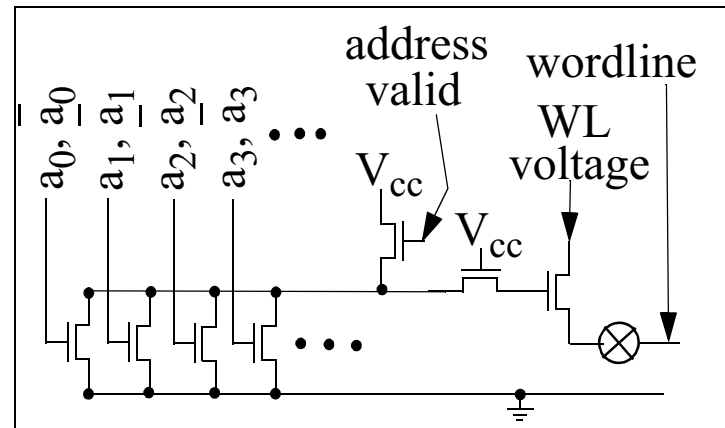


standard decoder (each row has one)

**functionally
equivalent to
NOR gate with
output that can
be disabled by
laser (or fuse)**
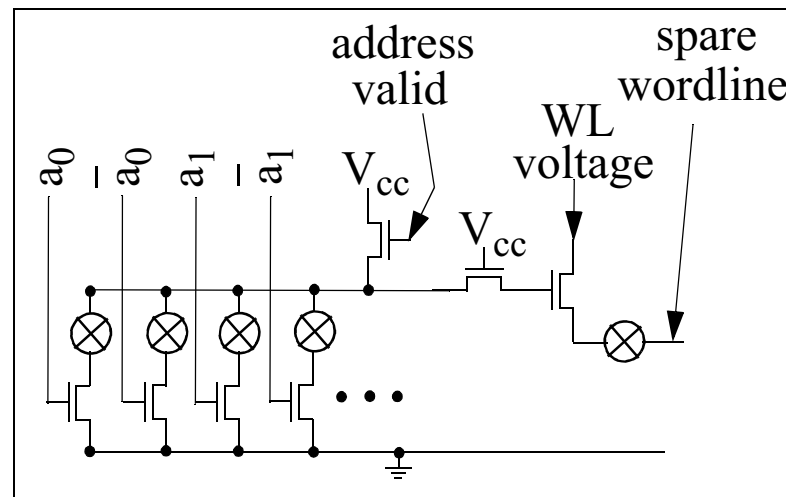
spare decoder (each spare row has one)

$\otimes$(laser) programmable link
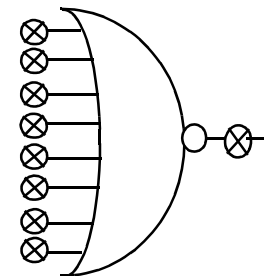
**functionally
equivalent to
NOR gate with
inputs that can
be selectively
disabled**

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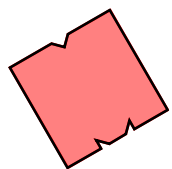
# Programmable Decoders II



4 address bits select 1 of 16 rows.
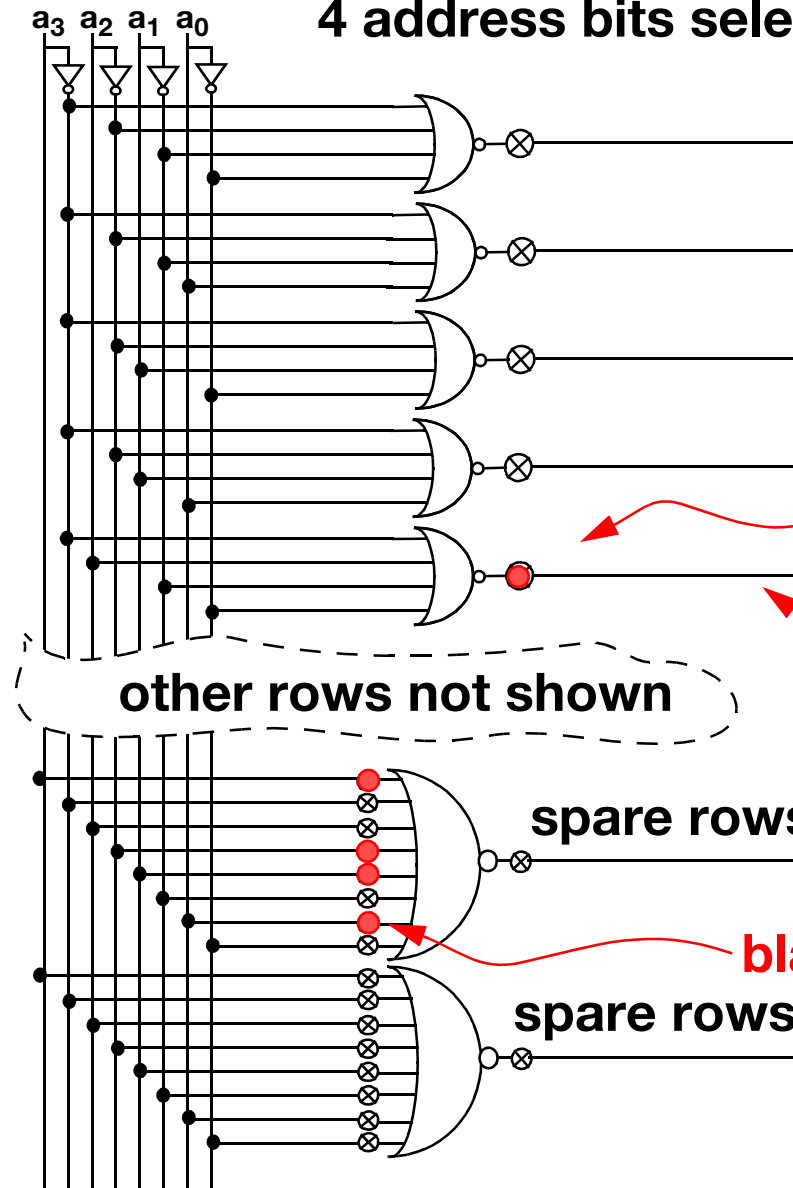
Suppose that row 0b0100 is defective.

blast it with laser

replace standard decoder with spare row decoder

other rows not shown

spare rows

blast it with laser

spare rows

$$\overline{\overline{a_3} + a_2 + \overline{a_1} + \overline{a_0}}$$

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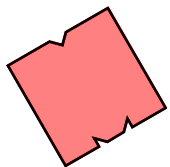
# Device Control Logic
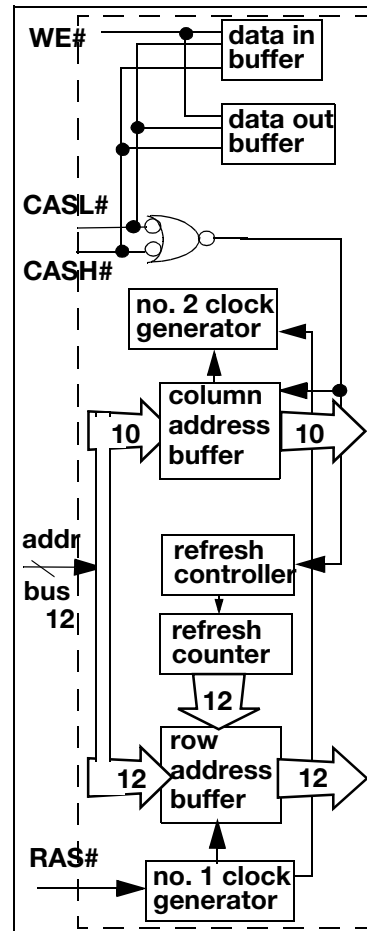


**SDRAM**

**Control Logic**

**FPM**
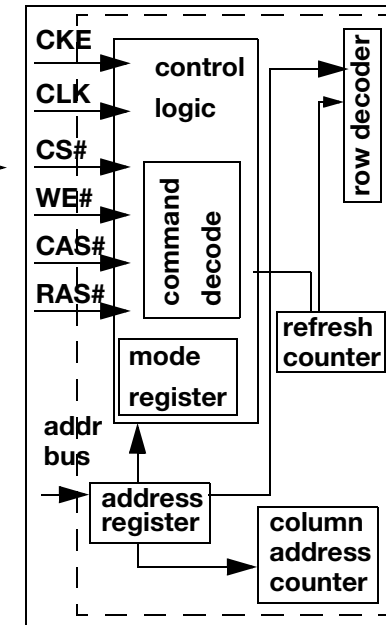
**Remember SAN and SAP?
Something has to control
sequence and timing**

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# Mode Register

CKE
CLK

**control logic**

CS#
WE#
CAS#
RAS#

**command decode**

**mode register**

12 11 10 9 8 7 6 5 4 3 2 1 0

**CAS Latency**      **Burst Type**      **Burst Length**

**Burst Length = 1, 2, 4, 8, or Page mode**

**CAS Latency = 2, 3 (4, 5, etc in special versions)**

**Burst Type = Sequential or Interleaved**

addr bus → **address register**

0 - 1 - 2 - 3 - 4 - 5 - 6 - 7      0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
1 - 2 - 3 - 4 - 5 - 6 - 7 - 0      1 - 0 - 3 - 2 - 5 - 4 - 7 - 6

**Modern DRAM devices (SDRAM, Direct RDRAM, DDRx SDRAM, etc. have programmable behaviour)**
**Load value from address bus with special command.**

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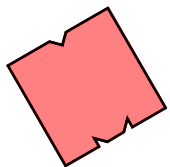
# Data I/O
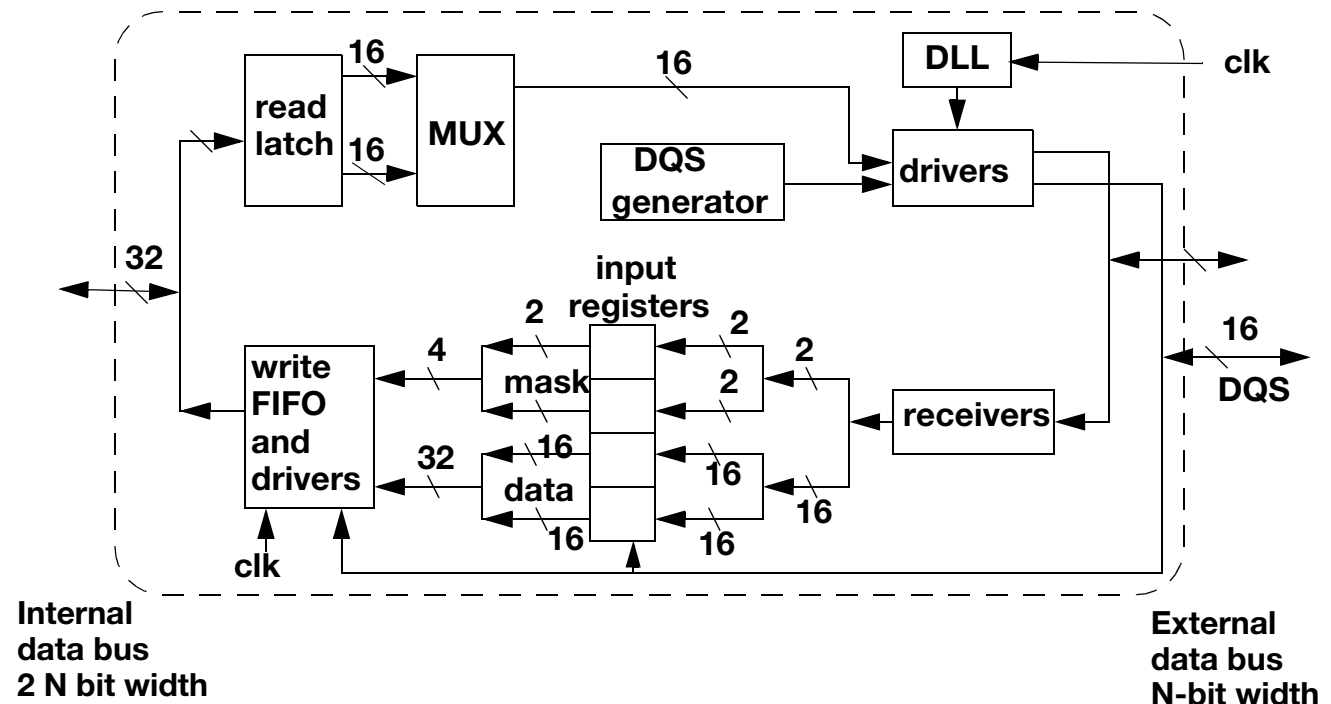


**2N Bit prefetch in DDR SDRAM devices**
**4N in DDR2 SDRAM devices, and**
**8N in DDR3 SDRAM devices**
**Allows "core" to run at slower datarates**
**while interface datarate cranks up.**
**drawback - minimum burst lengths**
**(loss of "randomness")**

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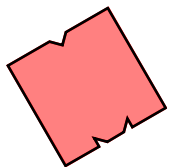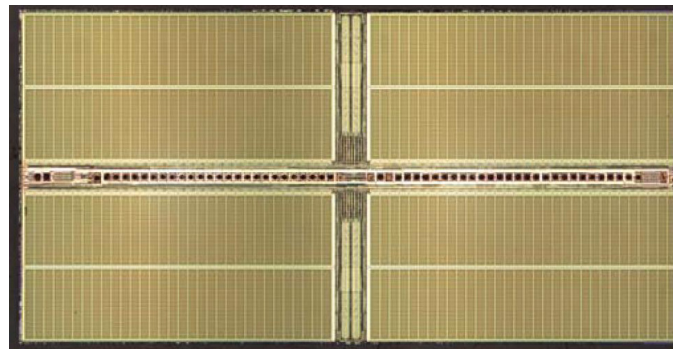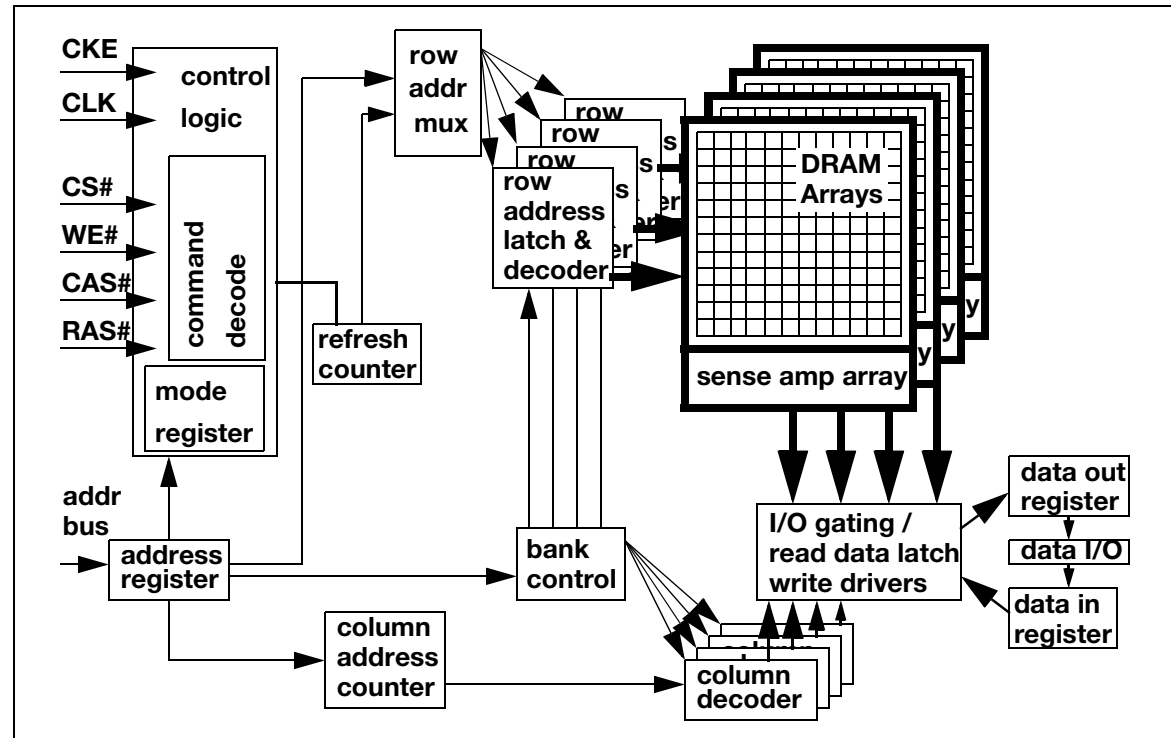
# SDRAM Device



Find bank 0, row 0x02F1, column 0x0EA and get an A

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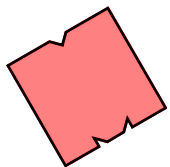
# SDRAM Evolution
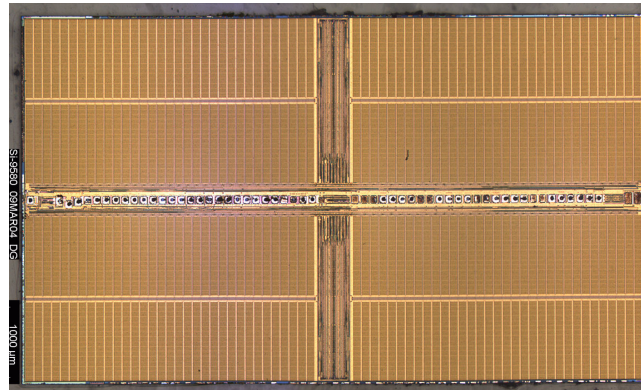
**Micron DDR1**
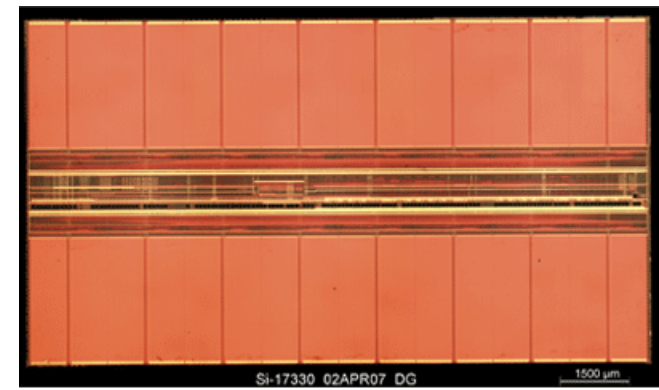
**Micron DDR3**

**Hynix DDR2**

**GDDR5**

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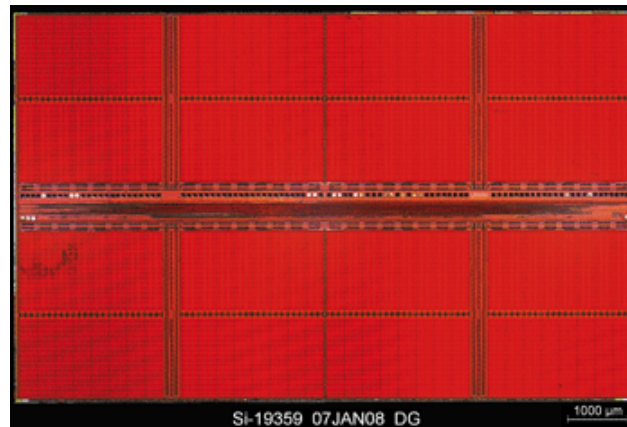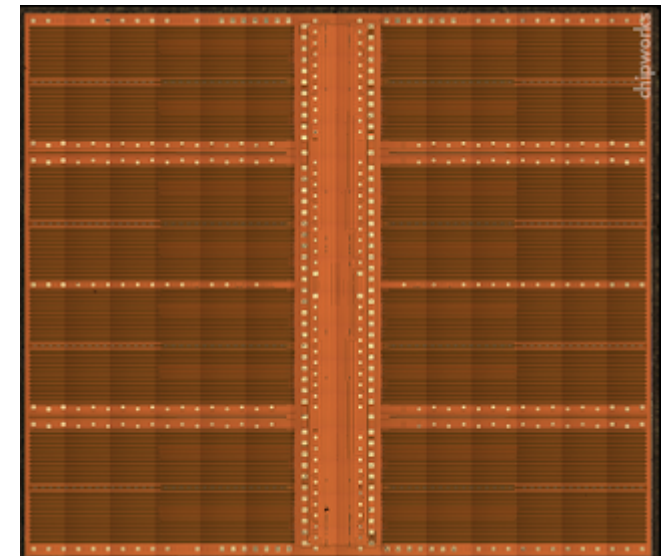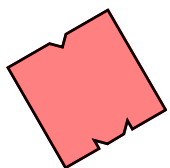
# Package and Pincount I

|  | 2011 | 2014 | 2017 | 2020 | 2023 |
|---|---|---|---|---|---|
| **High Perf. physical gate length (nm)** | 24 | 18 | 14 | 10.6 | 8.1 |
| **High Perf. device pin count** | 5094 | 5896 | 6826 | 7902 | 9148 |
| **High Perf. device cost (cents/pin)** | 0.97 | 0.83 | 0.71 | 0.61 | 0.52 |
| **Memory device pin cost (cents/pin)** | 0.22 – 0.42 | 0.20 – 0.36 | 0.20 – 0.30 | 0.20 – 0.26 | 0.19 – 0.25 |

## 2012 ITRS Roadmap



**DIP**          **SOJ**          **TSOP**          **BGA**
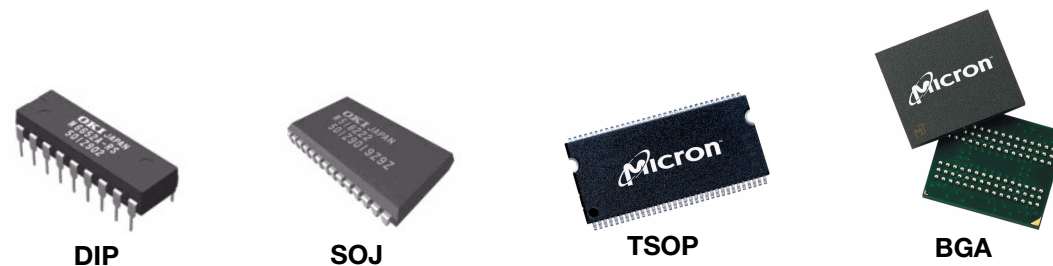
**Package Evolution
(higher pin count, higher datarate)
(higher costs, testing etc.)**

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# Package and Pincount II

16M x 16
32M x 8
64M x 4

| 16M x 16 | 32M x 8 | 64M x 4 | Pin | | Pin | 16M x 16 | 32M x 8 | 64M x 4 |
|---|---|---|---|---|---|---|---|---|
| VCC | VCC | VCC | 1 | | 54 | VSS | VSS | VSS |
| DQ0 | DQ0 | NC | 2 | | 53 | NC | DQ7 | DQ15 |
| VCCQ | VCCQ | VCCQ | 3 | | 52 | VSSQ | VSSQ | VSSQ |
| DQ1 | NC | NC | 4 | | 51 | NC | NC | DQ14 |
| DQ2 | DQ1 | DQ0 | 5 | | 50 | DQ3 | DQ6 | DQ13 |
| VSSQ | VSSQ | VSSQ | 6 | | 49 | VCCQ | VCCQ | VCCQ |
| DQ3 | NC | NC | 7 | | 48 | NC | NC | DQ12 |
| DQ4 | DQ2 | NC | 8 | | 47 | NC | DQ5 | DQ11 |
| VCCQ | VCCQ | VCCQ | 9 | | 46 | VSSQ | VSSQ | VSSQ |
| DQ5 | NC | NC | 10 | | 45 | NC | NC | DQ10 |
| DQ6 | DQ3 | DQ1 | 11 | | 44 | DQ2 | DQ4 | DQ9 |
| VSSQ | VSSQ | VSSQ | 12 | | 43 | VCCQ | VCCQ | VCCQ |
| DQ7 | NC | NC | 13 | | 42 | NC | NC | DQ8 |
| VCC | VCC | VCC | 14 | | 41 | VSS | VSS | VSS |
| DQML | NC | NC | 15 | | 40 | RESERVED | RESERVED | RESERVED |
| WE# | WE# | WE# | 16 | | 39 | DQM | DQM | DQM |
| CAS# | CAS# | CAS# | 17 | | 38 | CLK | CLK | CLK |
| RAS# | RAS# | RAS# | 18 | | 37 | CLKE | CLKE | CLKE |
| CS# | CS# | CS# | 19 | | 36 | A14 | A14 | A14 |
| A13(BA0) | A13(BA0) | A13(BA0) | 20 | | 35 | A11 | A11 | A11 |
| A12(BA1) | A12(BA1) | A12(BA1) | 21 | | 34 | A9 | A9 | A9 |
| A10(AP) | A10(AP) | A10(AP) | 22 | | 33 | A8 | A8 | A8 |
| A0 | A0 | A0 | 23 | | 32 | A7 | A7 | A7 |
| A1 | A1 | A1 | 24 | | 31 | A6 | A6 | A6 |
| A2 | A2 | A2 | 25 | | 30 | A5 | A5 | A5 |
| A2 | A2 | A2 | 26 | | 29 | A4 | A4 | A4 |
| VCC | VCC | VCC | 27 | | 28 | VSS | VSS | VSS |

54 pin
TSOP

## SDRAM "Same pinout", except for data bus

# Process Technology



Process Back End

Process Front End

2 layers of Al — **Metal Interconnections** — 7+ layers of Cu

$SiO_2$ — **Inter-layer Dielectric** — low K

layer of Tungsten

4+ layers:
cell capacitance — **Polysilicon** — 2 or 3 layers:
local interconnect

**Transistors**

high $V_t$:
leakage optimized — low $V_t$:
Drive current optimized

trench capacitors

bulk silicon — **Substrate** — BOX: Buried Oxide layer

**DRAM Optimized Process**          **Logic Optimized Process**