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VLSI Architecture for Orthonormal Wavelets Without Multipliers

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Abstract

The Discrete Wavelet Transform (DWT) is proving to be a highly effective tool in progressive coding of audio and video data. Due to the advances in ISDN network and high definition television (HDTV) technology, a high speed computation of the DWT has become very desirable. Since the algorithmic implementations on programmable DSP chips can not match the high throughput requirements of these applications, the use of specialized VLSI designs has emerged. The wavelet transform can be implemented by a tree structured digital filter bank. In particular, for an orthogonal wavelet basis this filter bank exhibits the paraunitarity property, thus it can be realized by using the Givens rotation as the basic building block. A complete parameterization for this class of systems is known.

In this paper, we consider the architectural implementation of the DWT that is associated with an orthonormal wavelet basis. We discuss the trade-offs involved in the use of distributed arithmetic and CORDIC processors for the implementation of the Givens rotation. The resulted circuits are modular, regular and they require only local communication. Furthermore, they involve only adders and ROM lookup tables and no multipliers. Consequently, they are very appropriate for VLSI implementation. The question of the on-line adaptation of the parameters of the circuit is also addressed. This feature is very important in adaptive signal processing applications. Although our discussion is focused on the one-dimensional dyadic DWT, our conclusions are projected to the M -band orthonormal wavelets and the two-dimensional DWT with quincunx subsampling.

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