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of High Power Surveillance T/R Modules

(with M. McMahon, R. Prasannappa, G. Zhang,
A. Kebede and P. Mendicino)

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EVALUATION OF PRODUCT AND PROCESS DESIGN IN ELECTRONICS [*]

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Abstract

This paper describes techniques and an implementation for managing costs and quality of electronics products during design. Emphasis is given to the development of an economic model to estimate the production costs at the assembly level. The unique feature of this system is to bring the experience of a manufacturing engineer, quality engineer, and cost controller into the hands of a designer. Such an early integration of manufacturing knowledge creates a concurrent engineering environment which improves product quality and reduces cost through careful monitoring of the design phase.

Introduction

Increasing global competition is challenging the U.S. manufacturing industry, especially electronics manufacturing, to bring competitively-priced, well-designed and well-manufactured products to market in a timely fashion. As the technology used in electronic parts continues to evolve, the tools used to support this development must similarly improve. The introduction of new components provides more choices for designers; new manufacturing processes and dynamic plant capabilities lead to alternative process plans; various specifications and physical constraints grow with these combinations. The theme of concurrent engineering is now spreading to the electronics industry to address these production management issues.

Automated planning systems are frequently used both to generate alternative routings for a particular assembly [ChTi88] and to improve the design. Once a feasible plan is formulated, an objective means should be available to evaluate the alternatives with respect to some prescribed goals. Possible goals might be performance, manufacturability [BaRe86], cost [Bo89], reliability, quality [Do83], or schedule [MaKa]. These measures are usually not independent, and require some degree of trade-off to find the desired balance. This paper emphasizes cost and quality as evaluation criteria, and discusses the representation of these two elements for use in a process planning system. The reader is referred to the cited works as exemplifying previous research in these areas.

The paper begins with a discussion of the basic approach to this problem, then a broad description of the overall implementation. This is followed by a more detailed development of the economic model and an introduction to the quality module under development. A case study is provided which demonstrated the benefits of this system. The software implementation is discussed, followed by conclusions.

Basic Approach

A product development cycle involves three fundamental design stages: the actual product, the manufacturing processes, and the production strategy. Experience with hybrid electrical-mechanical products at Westinghouse indicates that efficient design for manufacture occurs only when information flows through these three stages in a coordinated fashion. Traditionally design engineers, manufacturing engineers, quality engineers, and cost controllers approach the integrated product development cycle with differing, sometimes conflicting, views. The central idea of concurrent engineering is to bring the experience of these three disciplines into the hands of designers. In this way, manufacturing concerns may be addressed early in the design cycle at minimal cost impact.

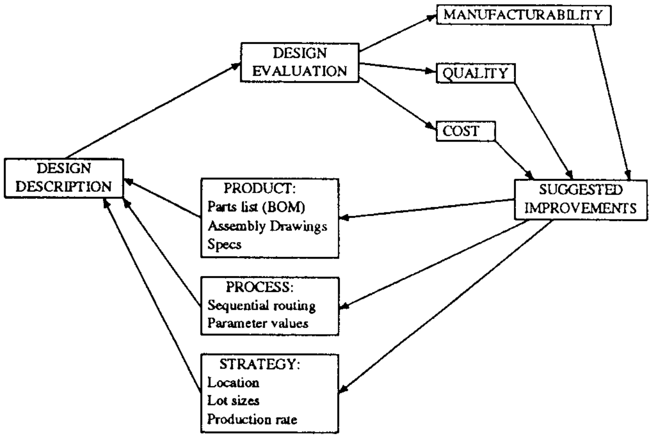

Figure 1: Concurrent Design.

Figure 1 gives an overall view of how the design, routing, and strategy are changed in a closed-loop, iterative design process. The product development starts with an initial design attempt, which includes preliminary drawings or sketches and a parts list. Based on this information, the production engineers determine the required sequence of manufacturing processes. Both the design and the resulting process plan are evaluated with respect to cost, quality, and manufacturability. The analysis is used to "critique" all three levels of concern in an objective manner. The results point out how the design might be changed to improve its manufacturability, reveal the combination of processes and process parameters which are most favorable, and suggest a strategy for most efficient use of production resources.

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System Architecture

The starting point in the system is a preliminary design description which may be nothing more than a parts list and rough layout sketch provided by design engineers. These data are entered into the system database by means of graphical panels, and a suitable process plan is then developed interactively by either of two methods. A plan may be retrieved from the knowledge-base according to similarities to an existing design; alternatively, a new process plan may be designed from scratch. In either case, the database augments the design description with process requirements and constraints to assist the planning module.

At this stage, the plan is guaranteed only to be feasible, not that cost is lowest, quality highest, nor manufacturability greatest. The planning module makes semi-intelligent decisions based on manufacturing information contained in the knowledge-base, but cannot hope to refine the design in a single step. Deficiencies will be resolved in the next stage, when three distinct models provide an objective evaluation of the product/process design.

The quality module is first to critique the output from the planner. According to the specific processes used, first-pass yield is estimated for this product based on historical data, process-parameters used, and specified tolerance levels. Revised parameter or tolerance values are suggested to the planner wherever process capability is exceeded, and scrap and rework estimates are sent to the cost model. The cost model is now invoked to estimate production costs under the current scenario. A third measure of design adequacy is manufacturability: this model, a truly independent measure based on weighted design attributes, is developed in a previous work [Ra92].

Having completed this evaluation, these results are used to refine both the product design and process plan. The problem is one of iterative refinement which is familiar to design engineers. While some of these refinements can be automated, the software does not displace the role of a knowledgeable human designer. Rather, the system is intended as a software tool used to enhance an engineer's productivity. Figure 2 demonstrates the role of these technologies in implementing the basic approach outlined above. One technology not shown is the graphical user interface, which promotes creative design by providing informative ways of viewing system data and results.

Internally, the system represents the manufacturing environment using a hierarchical, object-oriented model. This exploits similarities amongst processes, materials, and equipment to manipulate these data at a high level of abstraction— with a considerable savings of computer overhead. Design *constraints*, such as plant capabilities and component tolerances, are also represented in this fashion. The *assembly*, *process*, and *expense* types are other structures developed for storing comparative designs in progress. We emphasize the importance of suitable data representation, in both completeness and flexibility; process-planning is not well suited by a rigid data model. This also requires a suitable database technology for consistent mapping between volatile memory and long-term storage [St91].

Economic Model of Electronic Assembly

The cost model provides a general economic model of electronic assembly consisting of three major parts: a hierarchical assembly, process cost estimators, and a collection of generic cost elements (called "expenses"). An estimating system is developed in favor of an accounting system: at the design stage, order of magnitude approximation is preferred to allocability determination. This sub-system is now explained in detail, concentrating on structure and operation rather than explicit mathematical formulation.

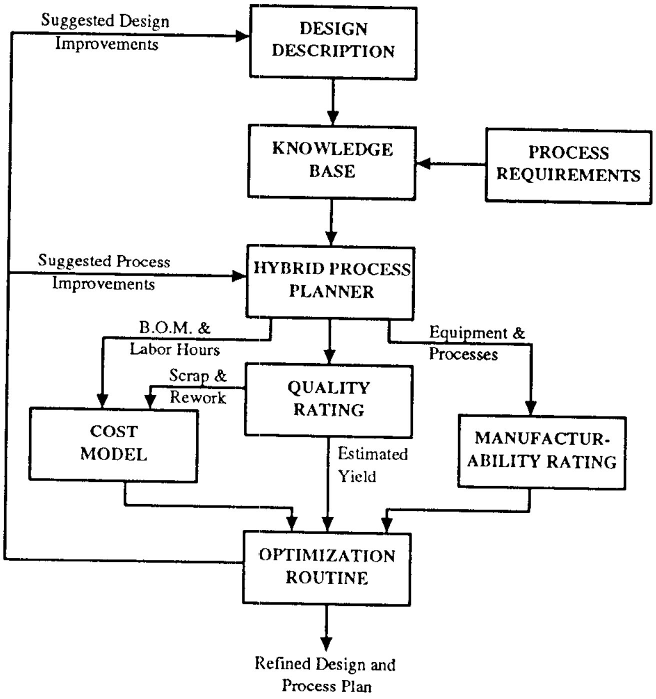


Figure 2: System Architecture.

Assembly Structure

Fundamental to the cost model is the existence of a hierarchical assembly to be estimated. As illustrated in Figure 3, engineered products are typically grouped into functional assemblies by related expense items. The top level assembly is composed of numerous sub-assemblies, on down to the component level, in a tree-like manner. A particular assembly contains information describing the parts used at this level, a list of required processes, its parent assembly, and constituent sub-assemblies. Consequently, the top level assembly depends on each of its siblings: the slightest change at a lower level propagates upwards, defining a unique assembly.

Based upon this definition, assembly costs draw from two main sources: the parts list and the process list. Assembly cost methods work by iterating over these two lists while calling the appropriate process or material methods, which are lower-level functions of greater detail. The assembly algorithm is now simply:

```
For each in (ProcessList, Bill of Materials):
        Invoke appropriate low-level cost function
        Keep running totals
```

Costs incurred at the current level are distinguished from those of sub-assemblies. The above method calculates costs of the current assembly level only: total assembly costs are found by recursively invoking this method for each sub-assembly.

Processes and Cost Estimators

The representation of a process plays an important role in the cost determination. Due to the great disparity in types of pro-

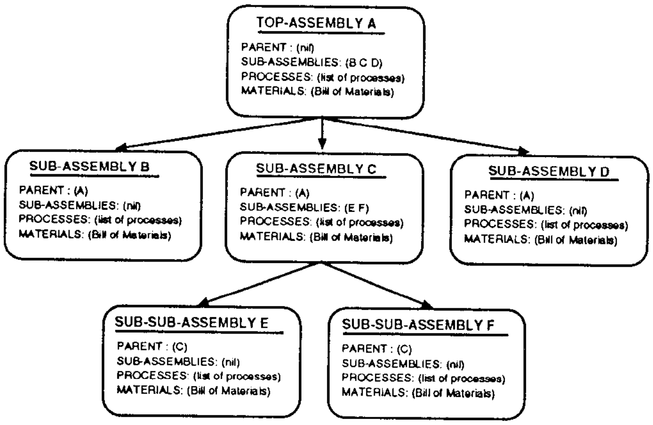


Figure 3: Assembly Hierarchy.

cesses, the nature of cost calculations is similarly varied. These process-specific details are contained in process level methods, thereby keeping the assembly methods generic and allowing a more detailed evaluation of the process at hand.

The database contains many cataloged processes which act as a "library" from which the planning module may select. Each process record has two sections: a shared part common to all processes of this type, and a private part unique in each occurrence. This design permits multiple instances of a given process with each invocation allowed separate data relevant only in its context; meanwhile, the common data is not duplicated. For example, each process has a list of possible successive processes which are always valid, while such parameters as conveyor speed and batch size will be unique in each instance. A default value and range of acceptable values is also stored for each parameter, but as shared data. This facility has obvious uses in the quality module as well. Completing the process definition are "local" process rules used to determine allowable conditions within a single process, and "global" rules used to decide use or disuse of this process.

Process cost estimator methods are developed to evaluate the cost elements of each individual process. Using both shared and private data, labor costs are calculated as explained further on. "Special" expense cases are handled at this level, for example, a wire-bonding process which uses expensive gold leads has more cost factors than point-to-point soldering. However, the external interface seen by the assembly methods is the same.

Cost is a planning consideration at two levels: locally (within a single process) and globally (within the sequence of all processes). In the local case, quality issues, such as reflow speed/temperature, will hopefully interact with cost concerns in a predictable manner. In the global case, the problem domain is completely discontinuous; for example, the usefulness of inspection depends on both preceding and subsequent operations. The process estimator methods are therefore invoked to resolve costs for a single process, while the planning module tries several such methods in an effort to refine the global plan.

Expense Types

The major cost components in the production of a general electronic assembly are labor, material, burden, and scrap expenses. In the present work, these are grouped in a layered, object-oriented fashion based on their similarities, and are referred to by the generic name *expense* at the highest level. The taxonomy of these expense types is shown in Figure 4.

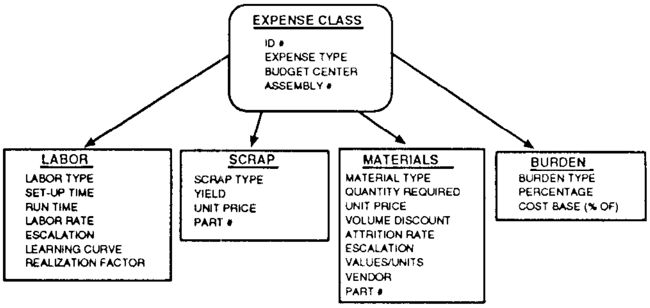


Figure 4: Expense Taxonomy.

Of these, labor, material, and scrap costs are the variable factors. Labor cost is strongly time-dependent: its function is to account for all measurable time spent by a paid operator. The workforce is divided into various classes of labor which perform unique functions for a certain wage. As these workers become more skilled over time, there will be a decrease in assembly time, while hourly wages usually increase. Overall labor costs therefore vary. The former effect dominates a short product development cycle, which the latter dominates longer production schedules. As a result, an exponential learning curve is used to dynamically adjust the total labor time and is given as follows:

$$T = t_0 \sum_{i=1}^{V} L_C^{\frac{\ln(i)}{\ln(2)}}$$

where T = total labor time, t_0 = initial labor time, V = volume produced, and L_C = learning curve, which is the fraction decrease for each doubling of V. The main variable here, L_C, follows the standard definition [Ma84] and reflects the operator "teachability". The summation results directly from this definition of L_C and it is not obvious that each iterate represents an exponential decrease in labor time (recall $L_C \leq 1$).

Material costs are used for all items purchased through outside sources, as listed in the Bill of Materials, or process raw-materials, as contained in the process estimator methods. Material costs are also subject to time adjustment: attrition and inflation are most common, while commodity items, such as memory chips, might decrease in price over time. By design, these details are hidden in low-level cost estimation methods, thereby simplifying the more generic external interface.

Scrap expenses are costs of non-conforming components resulting from unavoidable process variations. These defects can be either reparable or fatal. The former may be fixed, and the additional cost are sub-classed as *repair* expenses and calculated by the repair process methods. Parts with fatal defects must be scrapped, and the value added in previous steps is lost as a scrap expense.

The fixed costs of equipment, indirect labor, and miscellaneous overhead are included as burden because they are in general recurring costs. At the design stage, burden costs are usually difficult to assign with any precision, and so are estimated either from historical data or are allocated on a percentage basis of better known quantities, such as labor or material costs.

Quality Model

Methods have been developed to assess the first-pass yield of a given design and process plan. The general approach recognizes that each additional manufacturing operation has the potential to introduce defects into the product: these defects may be either reparable or fatal. Each of the main processes are studied to determine what types of defects may be caused and with what frequency. Process yield is determined both by the upper/lower specification limits and by the process variance. Therefore, yield may be improved either by expanding these limits or by reducing variability. As suggested by Taguichi, careful selection of the controlling process parameters can result in significantly reduced variability, with an accompanying increase in yield.

The quality model requires that relationships first be established between process parameters and one or more measurable output variables. Such variables are usually bounded by upper and lower specification limits: performance outside this range constitutes defective operation. There are several possibilities for establishing these relationships, such as a statistical approach, a heuristic approach, and a neural network approach. Only the first two are considered due to the larger scope of this project.

The standard statistical approach assumes a Gaussian distribution of dependent variables and calculates the standard deviation σ and mean $\bar{X}$ of this distribution [Mo85]. This method works well when historical data are readily available, and when there are few dependent parameters. With several parameters involved though, one must first isolate the dependent from the independent variables: this is most easily done using linear regression analysis. In operation, predicting process yield is straightforward using the determined σ and $\bar{X}$ and the current upper/lower specification limits. The area under the Gaussian curve between these limits gives percentage of good parts and is easily found by solving:

$$Y = \int_{LSL}^{USL} e^{[\frac{-(x-\eta)^2}{2\sigma^2}]}\,dx$$

where LSL/USL = lower/upper specification limit, and $\eta \equiv \bar{X}$. This area decreases as σ becomes larger- a reflection of poor variability - or the mean shifts- an indication of a more systematic problem.

These calculations are performed for each process, with the product of these giving overall first-pass yield. For most applications, this would be sufficient. However, the planning module must also consider the possibility of performing rework on defective parts. For each defect type a list is maintained of possible rework operations: a null list indicates a fatal defect which must be scrapped.

Case Study

The benefits of cost/quality analysis in an integrated planning system are best presented through a case study. The example considers a typical management dilemma: the development of a cost effective test/rework strategy. Figure 5 compares three ways of producing final Assembly A. Scenario 1 uses a strategy with no inspection until the final part is assembled. Using this strategy gives a unit cost of \$1501, lowest of the three. Taking into account an overall yield of 71%, the apparent cost for each good part (CGP) is really \$2111.

In Scenario 2, a 99% effective Inspection process is added which increases the unit cost to \$1529. The good news is that final yield has improved to 81% while CGP falls to \$1888. By identifying and removing the non-conforming parts early in production, a savings of 10% is realized for the good parts which remain. Inspection of Sub-Assembly C is justified due to the costs of further processing such a low-yield product as in Scenario 1.

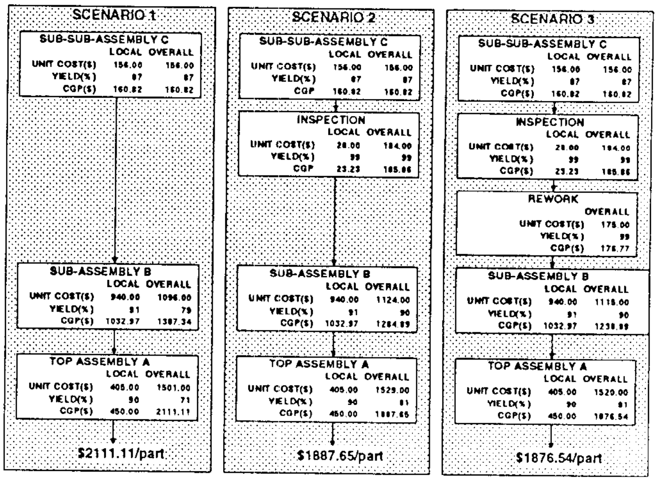


Figure 5: Cost vs. Yield Study. Overall cost reflects sum of subassembly local costs. Cost per good part (CGP) divides overall cost by overall yield.

Scenario 3 advocates repair of the defective parts which were previously scrapped in Scenario 2. This step does not increase overall yield, which remains at 81%, but the effective cost CGP is reduced to \$1877. These calculations assume good repair success of Sub-Assembly C (that is, a low fatal defect rate) which tends to reduce that assembly's overall unit cost as compared with Scenario 2. Rework of these defective parts is justified due to the value already added in previous steps.

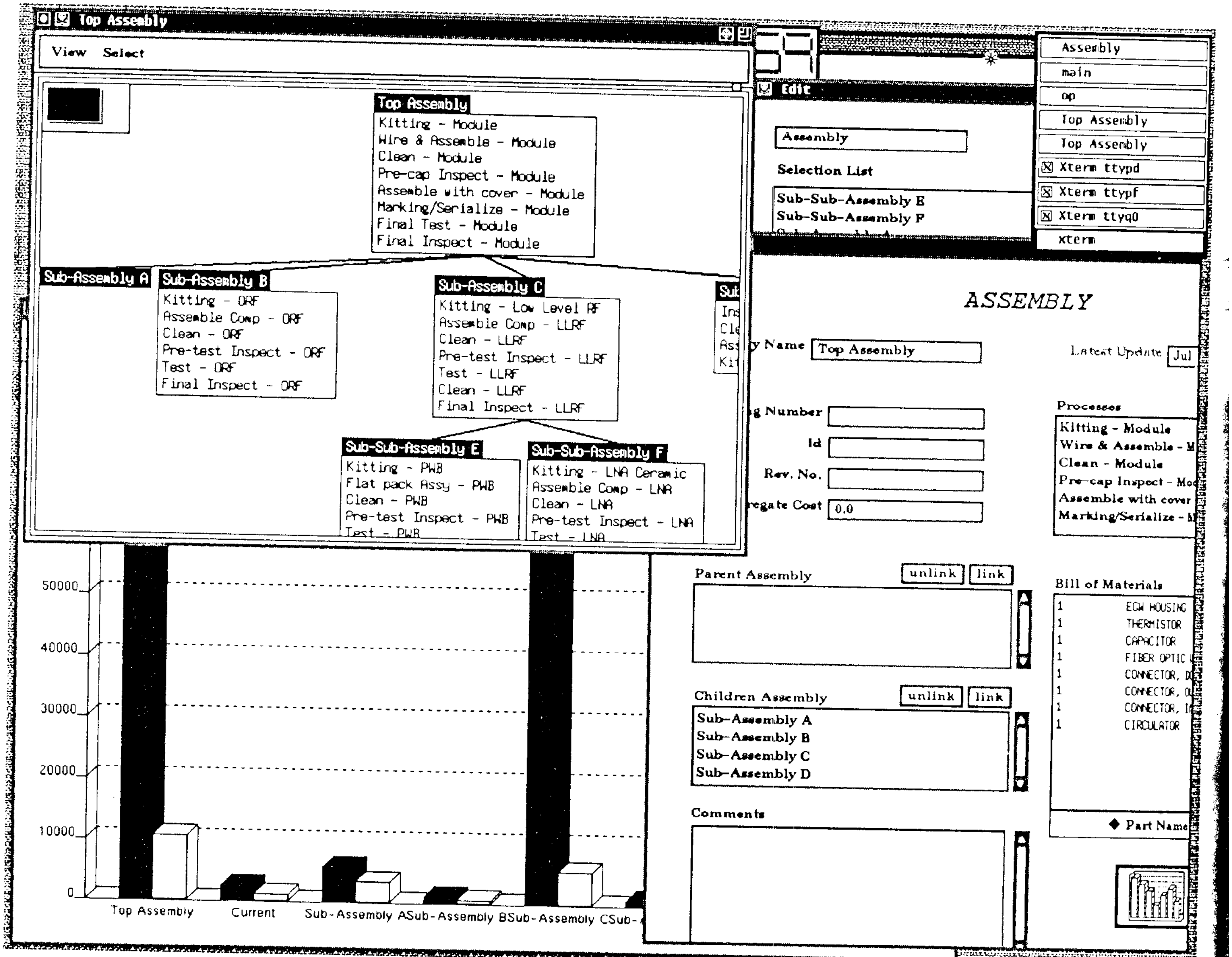
Several factors have conspired to produce these results. First, the low-yield assembly occurs early in the process flow, which tends to support inspection. Second, the inspection costs are a small percentage of the final assembly. Third, repairs are easily made to Assembly C- at low cost and with high success. And fourth, rework of Assembly A after final inspection is not considered and assumed to be prohibitively expensive. Changes to any of these parameters could affect the outcome of this study: scrapped parts are common in electronic manufacturing due to high rework costs. By quickly evaluating alternative design scenarios, this example presents the type of "what-if" analysis for which this software tool has been designed.

Implementation

The software implementation was developed in three stages: research of existing database and planning systems at Westinghouse, selection of available software subsystems, and customization of these items with current program needs. This research has benefited from previous Westinghouse works in process planning [ScSh82], quality control [Kl91], cost estimation, and manufacturability [Ra92]. In addition to published material, the engineers involved have provided valuable first-hand expertise in each of these areas.

Postgres, a next-generation database developed at University of California, Berkeley [St91], is used for permanent storage of program data. In addition to the features found in traditional relational database management systems, Postgres provides the sophisticated object and rule management capabilities required for this implementation. The graphical user-interface is developed using Transportable Application Executive (TAE+), a product of NASA. This interface builder utilizes Version 11 of MIT's X Window System and the Open Software Foundation's Motif Toolkit. Additional graphical *Widgets* have been programmed or purchased to provide a suite of reporting capabilities. Figure 6 demonstrates a sample hierarchical assembly, its resulting costs, and database input panels.

Again referring to Figure 2, several topics were developed specifically for this project and were described in this paper. Although much work remains, a prototype integrating these major system components has been successfully completed and is currently undergoing limited use at Westinghouse.



Top Assembly
- Kitting - Module
- Wire & Assemble - Module
- Clean - Module
- Pre-cap Inspect - Module
- Assemble with cover - Module
- Marking/Serialize - Module
- Final Test - Module
- Final Inspect - Module

Sub-Assembly A

Sub-Assembly B
- Kitting - ORF
- Assemble Comp - ORF
- Clean - ORF
- Pre-test Inspect - ORF
- Test - ORF
- Final Inspect - ORF

Sub-Assembly C
- Kitting - Low Level RF
- Assemble Comp - LLRF
- Clean - LLRF
- Pre-test Inspect - LLRF
- Test - LLRF
- Clean - LLRF
- Final Inspect - LLRF

Sub-Sub-Assembly E
- Kitting - PWB
- Flat pack Assy - PWB
- Clean - PWB
- Pre-test Inspect - PWB
- Test - PWB

Sub-Sub-Assembly F
- Kitting - LNA Ceramic
- Assemble Comp - LNA
- Clean - LNA
- Pre-test Inspect - LNA
- Test - LNA

Assembly

Selection List
Sub-Sub-Assembly E
Sub-Sub-Assembly F

ASSEMBLY

y Name: Top Assembly
Latest Update: Jul
g Number:
Id:
Rev. No.:
regate Cost: 0.0

Processes
Kitting - Module
Wire & Assemble - M
Clean - Module
Pre-cap Inspect - Mo
Assemble with cover
Marking/Serialize - M

Parent Assembly

Children Assembly
Sub-Assembly A
Sub-Assembly B
Sub-Assembly C
Sub-Assembly D

Comments

Bill of Materials

1	ECW HOUSING
1	THERMISTOR
1	CAPACITOR
1	FIBER OPTIC
1	CONNECTOR, D
1	CONNECTOR, O
1	CONNECTOR, I
1	CIRCULATOR

Figure 6: An Assembly Viewed by Process Hierarchy and Cost.

Conclusions

In this paper, an integrated system for evaluation of product and process design in electronics has been discussed. The importance of integrating cost and quality management to improve both product and process design has been demonstrated. Objective measures have been developed to aid in both comparison of alternatives and provide a baseline of progress. The estimation of cost and first-pass yield have been identified as the evaluation criteria most useful during the design stage. Application of these principles in an automated system can aid in realizing the true benefits of concurrent engineering. The system developed thus far is but a small step in that direction.

References

[Ar89] Arabian, Jack, "Computer Integrated Electronics Manufacturing and Testing, " Marcel-Dekker, Inc, NY, 1989.

[Ba88] Bao, Han P., "An Expert System for SMT Printed Circuit Board Design for Assembly,"*Manufacturing Review*, Vol. 1, No. 4., December 1988.

[BaRe86] Bao, Han P., and Reodecha, Manop, "An Approach to Appraising the Manufacturability of a Printed Circuit Board Assembly,"*First International Conference on Product Design for Assembly*, Proceedings, 1986.

[Bo89] Boothroyd, Geoffrey, "Estimating the Costs of Printed Circuit Assemblies," *Printed Circuit Design*, Vol. 6, No. 6, June 1989.

[BrBu88] Branceleoni, C., and Bugno, L., "Italsim: A Knowledge-Based Simulation of a PCB Manufacturing Plant,"*Fourth International Conference on Simulation in Manufacturing*, Proceedings, November 1988.

[Br88] Browne, Jack, "Microwave Substrates Lay the Groundwork for Hybrid Circuits," *Microwaves & RF*, January 1988.

[CaCi88] Cavalloro, Patrizia, and Cividati, Emanuela, "INCA: An Expert System for Process Planning in PCB Assembly Line," *Fourth IEEE Conference on Artificial Intelligence Applications*, Proceedings, March 14-18 1988.

[ChTi88] Chang, Tien-Chien, and Irizarry-Lopez, Vilma M., "Knowledge Based Process Planning for Electronic Assembly,"S*Second International Symposium on Robotics & Manufacturing: Research, Education, & Applications*, Proceedings, Nov. 16-18 1988.

[Do83] Dooley, Brian J., "A Model for the Prediction of Assembly, Rework, and Test Yields," *IBM Journal of research and Development*, Vol. 27, No. 1, January 1983.

[DrKl88] Driels, M.R. and Klegka, J.S., "Analysis of Printed Wiring Board Assembly Systems," *Fifth IEEE International Electronic Manufacturing Technology Symposium*, Proceedings, Oct. 10-12 1988.

[Ha64] Hartmeyer, Fred C., Handbook of Electronics Industry .Cost Estimating Data, John Wiley & Sons, 1964. Revised by Taylor, Theodore, 1985.

[Ke87] Kear, Fred W, Printed Circuit Assembly Manufacturing Marcel Dekker, Inc, NY, 1987

[Kl91] Kline, Michael D., "Achieving Total Quality Control in MIC's and MMIC's," *Microwaves & RF*, Nov. 1991.

[Ku88] Kusiak, Andrew, "Expert Systems and Optimization in Manufacturing," *Second International Symposium on Robotics & Manufacturing: Research, Education, & Applications*, Proceedings, Nov. 16-18 1988.

[MaKa] Mahanti, Ambuj, Karinth, R., Ghosh, S., and Pal, A., "AI Search for Minimum-Cost Set Cover and Multiple-Goal Plan Optimization Problems: Applications to Manufacturing, Planning, and Scheduling," (unpublished), West Virginia University, University of Maryland, and Indian Institute of Management.

[Ma84] Malstrom, Eric M., Manufacturing Cost Engineering .Handbook, Marcel Decker Publishing, 1984.

[Mo85] Montgomery, D.C., An Introduction to Statistical Quality Control, John Wiley and Sons, 1985.

[Na87] Nau, Dana S., "Automated Process Planning Using Hierarchical Abstraction", TI Technical Journal, Winter 1987.

[Ra92] Rathbun, Howard J., "Automated Manufacturability Evaluation for Microwave Modules", M.S. Thesis, University of Maryland, May 1992.

[ScSh82] Schwartz, S.J., and Shreve, M.T., "GT and CAPP: Productivity Tools for Hybrids," *International Journal for Hybrid Microelectronics*, Vol. 5, No. 2, 1982.

[St91] Stonebraker, Michael, and Kemnitz, Greg, "The Postgres Next Generation Database Management System", *Communications of the ACM*, Vol. 34, No. 10, October 1991.

[ZhLu90] Zhang, Guangming, and Lu, Stephen C-Y., "An Expert System Framework for Economic Evaluation of Operation Planning," *Journal of the Operational Research Society*, Vol. 41, No. 5, 1990.