The selective removal of metallic carbon nanotubes from As-grown arrays on insulating substrates

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We present a method of selectively removing metallic single-walled carbon nanotubes (SWCNTs) from as-grown arrays on quartz substrates. The process utilizes an external silicon piece as a temporary global top gate to increase the resistance of the semiconducting SWCNTs while current is passed through the metallic SWCNTs, causing electrical breakdown through joule heating. The resulting SWCNT field-effect transistors (FETs) consistently produce on/off current ratios greater than 1000. Additionally, we find that the high frequency parasitic losses between 1 GHz and 6 GHz on the completed SWCNT FETs are significantly lower than on comparable SWCNT FETs fabricated on silicon substrates. © 2012 American Institute of Physics. [http://dx.doi.org/10.1063/1.4765661]

The unique electronic properties of single-walled carbon nanotubes (SWCNTs) have made them a leading candidate for nanoelectronic devices. Common techniques for synthesizing SWCNTs (arc discharge,1 laser ablation,2 and chemical vapor deposition (CVD)3–6) produce a mixture of tubes which typically contain twice as many semiconducting tubes as metallic tubes.7 However, the presence of metallic SWCNTs in the active channel of a device can be problematic, producing a low on/off current ratio, typically near three for most as-grown SWCNT networks. For certain applications, a larger on/off ratio may be necessary for proper transistor operation. The presence of metallic tubes also means that an undesirable amount of current can leak through the channel even when the semiconducting SWCNTs are gated off. The inability of the transistor to be properly turned off means that appreciable power drain can arise, a concern for potential low power applications. One method of increasing the as-grown on/off ratio is to use low density (< 1 SWCNT/μm2) SWCNT random networks with channels of greater length than width.8 The more common solution is to selectively remove the metallic SWCNTs from as-grown networks.

The standard method to selectively remove metallic SWCNTs from a thin-film network is through gated electrical burnout in air.9–12 This is typically accomplished by utilizing a global back-gate on a silicon substrate to gate off the semiconducting SWCNTs as large currents are passed through the metallic SWCNTs. The resulting joule heating ultimately leads to the tubes being oxidized and then breaking.13 However, a silicon substrate may not be ideal for all device applications, particularly those requiring high frequency (HF) performance. Recent studies have characterized SWCNT performance in the microwave regime,14–17 allowing extrapolated cut-off frequencies in the tens to hundreds of GHz.18–22 In such applications, the same conductive silicon substrate that functions as a temporary global top gate. Our test structures also incorporate extended electrodes, allowing the removal of SWCNT from several channels simultaneously. The overall scheme, illustrated in Fig. 1, is divided into three stages. The first stage entails the formation of SWCNT channels and extended electrodes necessary for rapid removal from large areas. The second stage is the selective removal of metallic tubes with an external gate. The third stage is the completion of individual field-effect transistors (FET) with local gates.

Prior to fabrication, the quartz (device) and silicon (external gate) substrates are rinsed with acetone, methanol, and isopropyl alcohol, then blown dry with dry nitrogen to minimize adventitious particles and encourage conformal contact. The device channels consist of dense arrays of aligned SWCNTs grown by CVD on quartz substrates.11,22,24 Aligned arrays of SWCNTs are used to practically remove the resistive tube-to-tube contacts inherent to random networks of SWCNTs. Moreover, using the growth substrate as the device substrate means that the SWCNTs are exposed to less chemical processing than in solution deposition methods. The device electrode geometry is specific to high frequency characterization probes. Obviously, this selective removal process can be quickly extended over a whole chip. We next discuss in detail each stage of the process.

In stage I, the ground-signal-ground (G-S-G) geometry for HF probing is defined over an existing pattern of parallel array of SWCNTs (see Fig. 1(a)). The aligned SWCNTs are grown on ST-cut quartz wafers by CVD at 900°C with a ferri-tin catalyst deposited by dip coating. SWCNT channels (shown in Fig. 1(b)) are defined with lithographic oxygen
reactive ion etching (Plasma Therm RIE 790, 10 s, 200 mTorr, 100 W, 16 sccm of O₂). The resulting SWCNT film density is 1–3 tubes/μm of channel width. The over-layer of G-S-G electrodes, similar to other published high frequency electrode patterns, is composed of 100 nm of gold over a 5 nm titanium adhesion layer. The electrode thickness is chosen to create an air gap in the channel to facilitate electrical breakdown. Only the channel length (10 μm) and width (100 μm) are defined at this point, yet the G-S-G electrodes extend over five dual channels (four are shown in Fig. 1(a)). This superstructure allows burning to occur over a larger length scale. We note that the outer G-electrodes will become the source electrodes in the completed transistor while the inner S-electrode will become the drain electrode. Although not shown explicitly, the electrodes also extend several millimeters away from the channels to allow probing while the external top gate is in place.

In stage II, the selective removal process (shown in Fig. 1(c)) occurs. This is accomplished by bringing the external top gate in contact with the stage I electrodes. This global top gate consists of a piece of silicon (100 μm thick) in contact with the stage I electrodes. This global top gate is removed once the selective removal process is complete. The final device structure is obtained by truncating the G-S-G electrodes to create five individual units from the initial electrode geometry. Device isolation is accomplished by a chemical etchant for gold, while the titanium adhesion layer is removed with reactive ion etching (Plasma Therm RIE 790, 60 s, 40 mTorr, 175 W, 18 sccm CHF₃, 2 sccm O₂) as shown in Fig. 1(d).

The local gate dielectric layer is formed with 75 nm of atomic layer deposited alumina that is lithographically patterned in a buffered oxide etch. Finally, local top gates for the now-buried SWCNT channels are formed with 50 nm of atomic layer deposited alumina that is lithographically patterned in a buffered oxide etch.

Fig. 2 shows the output and transfer curves for two individual SWCNT FETs. The first device shown in Fig. 2(a) consists of an as-grown SWCNT network for the active channel, whereas the second device shown in Fig. 2(b) is a completed stage III device. By selectively exposing the metallic SWCNTs, the resulting on/off ratio is increased from the typical as-grown value near 3 to over 10 000 for a stage III device. This increase of nearly four orders of magnitude suggests that the metallic SWCNTs have been effectively removed. In addition, the output characteristics of completed stage III device clearly exhibit the desired field effect. We note that direct comparison of the same device before and after the selective removal process is not possible because 5 devices are electrically connected in parallel before the removal process. Moreover, a local gate is necessary for effective gating which is not possible prior to stage III, when the SWCNTs are buried under dielectric and gate layers. The two devices shown in Fig. 2 were on the same chip, and are representative of others of the same type.

As is common with gated electrical breakdown, the on-state conductance remains fixed at 50 V. This gives a total of 60 iterations that achieve a specific reduction in channel conductance while the external top gate is in place. Effective gating which is not possible prior to stage III, when the SWCNTs are buried under dielectric and gate layers. The two devices shown in Fig. 2 were on the same chip, and are representative of others of the same type.
leaving all semiconducting SWCNTs intact. Instead, we conclude that some semiconducting SWCNTs are also removed by the process. The unintended removal of semiconducting SWCNTs can be due to several causes such as variation in contact resistances for each SWCNT, screening of the gate field by charge defects and adjacent SWCNTs, and the chirality-dependent breakdown temperature. Moreover, in a parallel array, the presence of a highly resistive metallic SWCNT can result in semiconducting SWCNTs reaching breakdown even if effectively gated off. Thus, many semiconducting SWCNTs can be lost prior to the removal of a resistive metallic SWCNT. The practical consequence is that the output impedance of a completed stage III device is effectively increased as a result of the removal process. We also note that if a large on-state conductance is necessary for a given application, larger source/drain electrode widths with a higher number of SWCNTs initially could be used or the selective removal process could be terminated at a lower source-drain voltage.

To verify that the external top gate does affect the selectivity of metallic SWCNTs, the same procedure is repeated on five devices connected in parallel on a separate chip without using an external top gate. The source-drain voltage is increased from 25 V to 40 V as before, and then the devices are separated and completed. The resulting on/off ratios vary from 10 to 2000. It seems that even without a gating field most of the SWCNT with metallic character experience electrical breakdown at lower currents than most SWCNT of semiconducting character. However, the wide range of on/off ratios clearly shows that the metallic SWCNTs experience electrical breakdown at lower currents than most SWCNT of semiconducting character. We find that when an external top gate is used during the removal process; all of the resulting completed devices demonstrate on/off ratios greater than 1000, confirming that even a weak coupling between the gate and conduction channels ensures that at least some of the semiconducting SWCNTs are preserved. The result is that completed device on/off ratios can be reliably increased to practical levels.

Last, we compare the high frequency response of a completed stage III device on quartz with an aligned-SWCNT FET on Si/SiO₂ (300 nm thermal oxide). The aligned-SWCNT FET on silicon is fabricated by transferring the aligned tubes from a quartz growth substrate to a silicon device substrate. The electrode geometry (G-S-G) for this silicon device is the same as shown in Fig. 1(d). For the comparison, two-port scattering parameters (S-parameters) are measured from 1 to 6 GHz with a vector network analyzer (Agilent E5071C) with the signal from port 1 connected to the gate of the FET, and the signal from port 2 connected to the drain. The source electrodes are grounded through contact with the outer electrodes of the G-S-G probes (i.e., common-source configuration). Note that these measurements are taken with a local top gate, not the global silicon gate, and are calibrated to the plane of the G-S-G probes. The S-parameters can be used to quantify the losses at each port, and here they are used to extract the loss at port 2 as $\Delta_{\text{ds}} = 1 - |S_{12}|^2 - |S_{22}|^2$. Fig. 3 illustrates the extracted losses $\Delta_{\text{ds}}$ from 1 to 6 GHz of a completed stage III SWCNT FET on quartz and an aligned-SWCNT FET on silicon. As expected, $\Delta_{\text{ds}}$ for the silicon device is clearly greater than the $\Delta_{\text{ds}}$ for the completed stage III device on quartz over the frequency range measured. We find that for the silicon device $\Delta_{\text{ds}}$ increases steadily from about 0.1 ($f = 1.1$ GHz) to 0.8 ($f = 6.0$ GHz), where the loss is nearly twice as much as the loss ($\Delta_{\text{ds}} = 0.4$) for the completed stage III device. The bigger loss for the device on silicon is likely due to the parasitic interaction with the Si back-plane. Thus, assembling a SWCNT FET on quartz minimizes the losses in this frequency range. Fig. 3 also illustrates that the selective removal procedure outlined here can further decrease the losses on quartz. We find that...
$\Delta_{ds}$ is nearly uniformly lower in this frequency range for the completed stage III device than for the $\Delta_{ds}$ of an as-grown SWCNT device on quartz. Thus, the selective removal procedure outlined here not only increases the on/off ratio but it also can decreases the HF losses in the frequency range measured here.

We have described a method for the selective removal of metallic SWCNTs from as-grown arrays on insulating (quartz) substrates. The procedure is performed simultaneously on five devices connected in parallel with an extended electrode configuration (compatible with high frequency probes) and an external temporary global gate electrode. After removing the metallic SWCNTs through oxidative burn-out, the parallel devices are then separated and truncated into five completed FETs with local top gates. The resulting SWCNT FETs consistently produce on/off ratios greater than 1000. However, there is a trade-off between the on-state conductance and the on/off ratio. We find that the on-state conductance decreases from approximately 100 $\mu$S to 10 $\mu$S as the on/off ratio is increased to practical levels ($>10^3$). Nevertheless, the losses in the high frequency range (1 to 6 GHz) of the completed devices on quartz are significantly improved in comparison with as-grown SWCNT FETs on silicon. The procedure presented here is robust and can be scaled to wafer-sized processes. It is also general enough to be used with other insulating substrates. Furthermore, high on/off SWCNT FETs can be fabricated on substrates that are more compatible with high frequency applications than silicon, and thus enabling potential low power SWCNT FET technology in the high frequency regime.