On the Design Parameters of Flip-Chip PBGA Package Assembly for Optimum Solder Ball Reliability

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Abstract—An experimental investigation of the warpage of a flip-chip plastic ball grid array package assembly is presented and a critical deformation mode is identified. The experimental data, documented while cooling the assembly from the underfill curing temperature to -40 °C, clearly reveal the effect of the constraints from the chip and the PCB on the global behavior of the substrate. The constraints produce an inflection point of the substrate at the edge of the chip. An experimentally verified three-dimensional (3-D) nonlinear finite element analysis proceeds to quantify the effect of the substrate behavior on the second-level solder ball strains. An extensive parametric study is conducted to identify the most critical design parameter for optimum solder ball reliability.

Index Terms—Far infrared Fizeau interferometry, flip-chip plastic ball grid array package, nonlinear FEM analysis, shadow moiré, solder ball reliability, warpage.

I. INTRODUCTION

FLIP-chip technology has been extended to various organic chip carriers by the improvement afforded by the underfill technique [1]–[3]. The flip-chip plastic ball grid array package (FC-PBGA) has numerous advantages over the conventional ceramic chip carrier packages. They include lower processing cost, lower dielectric constant, enhanced board-level solder ball reliability, etc. Flip chip solder interconnects on organic substrates have high potential as a pervasive packaging technology in industry as noted in National Technology Roadmap for Semiconductors (NTRS) [4].

In the FC-PBGA package, the chip is placed active face downwards and the electrical connection between the chip and the chip carrier (or the substrate) is achieved by small solder bumps. The package is mounted on a printed circuit board (PCB) by larger solder balls to form a final assembly.

When the assembly is subjected to a temperature excursion, the deformation of the substrate under the chip is constrained by the chip through an underfill layer, while the deformation of the rest of the substrate is constrained by the PCB through the solder balls. Since the chip has a much lower coefficient of thermal expansion (CTE) than the PCB, the degree of constraint on the substrate is different. As a result, the maximum strain occurred at the solder ball located at the edge of the chip [5].

The purpose of investigation conducted in this work is to contribute to the understanding of the effect of the package warpage on solder ball strains. Extensive research has been performed to investigate the effect of warpage on reliability of PBGA packages and substrates [6]–[9]. However, only limited information is available in the literature regarding the effect of warpage on the second level solder ball reliability.

In this work, two full field warpage measurement techniques are employed to document thermally-induced warpage of a FC-PBGA package and its assembly. The results corroborate an earlier work by the authors [5], where a FC-PBGA package assembly with a strip configuration was analyzed by moiré interferometry. The strip contained only a few central rows of solder balls, but faithfully revealed the behavior of the package assembly. A 3-D nonlinear finite element analysis (FEA) is followed to quantify the effect of the substrate deformation on the solder ball strains. An extensive parametric study is conducted to identify the most critical design parameter for optimum solder ball reliability.

II. EXPERIMENTAL CHARACTERIZATION

A. Experimental Method

Two interferometric techniques were employed in the experimental investigation: far infrared Fizeau interferometry (FIFI) and shadow moiré with enhanced sensitivity (SMES) [10]. Far infrared Fizeau interferometry is an optical method that provides a whole-field map of surface topography. The method retains the simplicity of the classical Fizeau interferometry while providing a wide applicability to dielectric rough surfaces. With a far infrared light of CO₂ laser (λ = 10.6 μm), the basic sensitivity provided by the method is 5.3 μm per fringe order.

Shadow moiré also provides whole-field maps of out-of-plane displacements but with relatively coarse sensitivity (typically 25 to 50 μm per fringe order). Shadow moiré with enhanced sensitivity is based on shadow moiré but utilizes the optical/digital fringe multiplication (O/DFM) method [11] to increase the sensitivity beyond the practical limit of shadow moiré. In both methods, the relationship between the out-of-plane displacement W and fringe order N₂ is

\[ W = CN₂ \]  

(1)
where \( C \) is a constant that defines a contour interval of the fringe patterns.

A compact apparatus integrating the two techniques is illustrated schematically in Fig. 1. It is based on a computer controlled environmental chamber. The chamber has a heating/cooling rate of 0.5 \( ^\circ \)C/sec. and an operating range of \(-50 \) to \( 300 \) \( ^\circ \)C. The specimen is mounted on a special fixture (not shown) located inside the environmental chamber, which in turn is connected to flexible shafts. The flexible shafts permit the necessary adjustment of the specimen while operating the environmental chamber. By combining the two methods, the apparatus provides unique capability of thermally induced warpage measurement with variable sensitivity, ranging from 5.3 \( \mu \)m to 100 \( \mu \)m. The detailed optical and mechanical configuration of the apparatus can be found in Ref. [10].

B. Package Assembly Configuration

The cross-sectional view of the FC-PBGA package and its assembly is depicted schematically in Fig. 2 with relevant dimensions given. In the assembly, a silicon chip (6.9 \( \times \) 6.1 \( \times \) 0.76 mm) was attached to an organic substrate through eutectic solder bumps. The gap between the chip and the substrate was filled with an epoxy underfill to reduce the strains in the solder bumps. The substrate consisted of a BT core and build-up structures [12]. The total thickness of the substrate was 1.02 mm (0.040 in). The final dimension of the package body was 21 mm by 25 mm, which provided 304 I/O connections. The package was surface-mounted on an FR4 PCB (1.37 mm or 0.054 in thick) using larger eutectic solder balls.

C. Results and Implications

The FC-PBGA package and its assembly were installed in the environmental chamber. Initially, they were heated to the underfill curing temperature (140 \( ^\circ \)C). Then, the deformation of the chip side was documented by FIFI while cooling the specimens to \(-40 \) \( ^\circ \)C. The resultant fringe patterns at 140 \( ^\circ \)C and \(-40 \) \( ^\circ \)C are shown in Fig. 3(a) and (b) for the package and the assembly, respectively, where the contour interval is 5.3 \( \mu \)m per fringe order.

It is important to note that FIFI produced the fringe patterns on the surfaces of the chip and the substrate simultaneously, which are not in the same plane. The visible surface of the silicon is separated from the substrate plane by the thickness of the chip and the underfill. Nevertheless, the interferometric na-
ture of FIFI allowed the system to receive the information from both surfaces. In addition, the high contrast of the fringe patterns clearly indicates the effectiveness of FIFI to measure warpage of rough surfaces [13].

As expected, the chip was nearly flat at the underfill curing temperature and the warpage of the chip increased as temperature decreased. It should be noted that the underfill provides a strong coupling between the chip and substrate at low temperatures and thus the warpage of the chip should be nearly identical to the warpage of the substrate under the chip (will be referred as chip shadow region), as seen in the previous results of the cross-sectional moiré experiments [5].

More striking results were observed in the substrate warpage. The warpage of the substrate in the package increased as temperature decreased [Fig. 3(a)]. Note that the asymmetry seen in Fig. 3(a), however, the warpage of the substrate in the assembly was nearly zero at 140 °C and it remained unchanged during the entire cooling process for the portion of substrate, which was not under the chip (will be referred as bare substrate region).

In the package, the substrate in the chip shadow region was constrained through the underfill layer resulting in a large bending. However, the out-of-plane displacements of the bare substrate region was not produced by the constraints. Instead, they represent displacements caused by rigid body rotations; that is, the bare substrate region rotated rigidly due to the bending of the chip shadow region during the cooling process. After the package was assembled on the PCB, however, the bare substrate region was constrained by the PCB through solder balls while the constraints of the chip shadow region from the chip was maintained.

The changes in the chip and bare substrate warpage were extracted from the patterns in Fig. 3(a) and (b) and the results are plotted in Fig. 4. The effect of the PCB constraints in the assembly is evident. The warpage change of the substrate in the assembly induces a sudden change of curvature at the end of the chip shadow region (see inflection points in Fig. 4).

The deformation of the PCB side of the assembly was also documented to investigate the warpage behavior of the PCB. Shadow moiré with enhanced sensitivity was employed for the measurements since the metal pads on the PCB side produced uneven reflections of the infrared light and visibility of fringe patterns produced by FIFI was greatly reduced. The results are shown in Fig. 5(a), where the contour interval is 12.5 μm per fringe order. The change in the warpage of the PCB were extracted from the fringe patterns and plotted in Fig. 5(b) together with the substrate warpage from Fig. 4. Unlike the substrate, the warpage of the PCB changed uniformly and no inflection point was observed at the edge of the chip shadow region. The effect of the constraints from the chip on the PCB deformation was not as significant as their effect on the substrate. The larger bending stiffness provided by the thicker PCB also contributed to the uniform curvature.

The substrate is connected to the PCB through the solder balls and the curvature difference between the substrate and the PCB must be compensated by the deformation of the solder balls. The sudden change of the substrate curvature would produce large normal strains within the solder ball located at the inflection point. A numerical study was conducted to quantify the effect on solder ball strains.

III. NUMERICAL ANALYSIS

A. Finite Element Model

Three-dimensional nonlinear finite element analyses were conducted to determine the maximum solder ball strains. ANSYS V5.4 was used for preprocessing, solution and post-processing. The 3-D FEA mesh used in the analysis is shown.
Fig. 5. (a) Warpage contours of the PCB side obtained by shadow moiré with enhanced sensitivity and (b) changes in PCB warpage along the vertical centerline. The contour interval in (a) is 12.5 μm per fringe.

Fig. 6. Three-dimensional FEA model.

in Fig. 6, where only one-eighth of the assembly was modeled, taking advantage of the symmetry of the assembly. The solder balls were modeled as elasto-plastic solid and all other materials in the assembly were assumed to be linear elastic.

The temperature dependent nonlinear properties of the solder [14] and the linear elastic properties of the other materials used in the model are summarized in Tables I and II. The CTE and E values were obtained experimentally using moiré interferometry and a universal testing system. In the FEA model, the solder bump/underfill layer was assumed to be homogeneous to reduce the complexity of the model.

In order to verify the validity of the 3-D model, the warpage displacements of the substrate obtained from the FEA model were compared with the experimental data extracted from the fringe patterns in Fig. 3. The results are plotted in Fig. 7. The numerical prediction agrees very well with the experimental data. Accordingly, the specified boundary conditions and material properties were deemed appropriate for the subsequent analysis.

### Table I

<table>
<thead>
<tr>
<th>Temp.</th>
<th>-12°C</th>
<th>60°C</th>
<th>110°C</th>
</tr>
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<tbody>
<tr>
<td>E (GPa)</td>
<td>7.92</td>
<td>5.85</td>
<td>4.55</td>
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<table>
<thead>
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<th>Strain Stress (MPa)</th>
<th>Stress (MPa)</th>
<th>Stress (MPa)</th>
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<tr>
<td>5.0E-04</td>
<td>4.0</td>
<td>2.9</td>
</tr>
<tr>
<td>2.0E-03</td>
<td>13.4</td>
<td>9.4</td>
</tr>
<tr>
<td>6.0E-03</td>
<td>35.5</td>
<td>22.8</td>
</tr>
<tr>
<td>1.0E-02</td>
<td>52.3</td>
<td>32.8</td>
</tr>
<tr>
<td>2.0E-02</td>
<td>86.1</td>
<td>53.1</td>
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### Table II

<table>
<thead>
<tr>
<th>Material</th>
<th>E (GPa)</th>
<th>Poisson’s Ratio</th>
<th>CTE (ppm/°C)</th>
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<tr>
<td>Chip</td>
<td>186.0</td>
<td>0.30</td>
<td>3.2</td>
</tr>
<tr>
<td>Underfill/C4</td>
<td>10.3</td>
<td>0.33</td>
<td>24.0</td>
</tr>
<tr>
<td>Substrate</td>
<td>18.0</td>
<td>0.12</td>
<td>18.5</td>
</tr>
<tr>
<td>Copper</td>
<td>45.5</td>
<td>0.30</td>
<td>17.6</td>
</tr>
<tr>
<td>Solder</td>
<td>-</td>
<td>0.29</td>
<td>22.0</td>
</tr>
<tr>
<td>PCB</td>
<td>16.6</td>
<td>0.12</td>
<td>16.0</td>
</tr>
</tbody>
</table>

Fig. 7. Out-of-plane displacements obtained from the fringe patterns in Fig. 3 are compared to the numerical predictions.

B. Effect of Substrate Warpage

As discussed earlier, the uneven warpage of the substrate in the assembly was caused by the constraints from the chip and
The effect of the warpage on solder ball strains was investigated. The FEA model, geometrically identical to the specimen shown in Fig. 2, was subjected to a thermal loading of $\Delta T = -165 \, ^\circ C$ (cooling it from 125 $^\circ C$ to $-40 \, ^\circ C$). The maximum equivalent plastic strain (EQPS) of each solder ball was determined, and the result is plotted in Fig. 8. The third solder ball located at the edge of the chip has the largest strain and its magnitude is significantly higher than those of the other solder balls. The strains of the solder balls in the bare substrate region (solder ball no. 5 to 9) remain almost unchanged regardless of the distance from the neutral point (DNP).

The strain components of the point of the maximum EQPS explain the effect of the inflection point quantitatively. As can be seen in Fig. 9, the magnitude of normal strain in the thickness direction ($\varepsilon_z$) is much larger in magnitude, compared with other strain components. As discussed earlier, it was ascribed to the fact that the solder ball at the chip edge absorbed the deformation caused by the curvature difference between the substrate and the PCB. In the following section, an extensive parametric study on the FC-PBGA package assembly is presented to investigate the effect of design variables on solder ball reliability.

### C. Parametric Study

Three design variables were considered in the parametric study. They include the chip size, the substrate CTE, and the substrate thickness. Three values were chosen for each variable and they are shown in Table III. A total of 27 cases were analyzed. The thicknesses of the chip and the PCB were fixed at 0.76 mm and 1.37 mm, respectively. The maximum EQPS occurred at the solder ball located at the edge of the chip for all the cases. The magnitude of the maximum EQPS was determined for each case and the results are shown in Table IV. It is to be noted that the Young’s modulus of the substrate was kept constant for all cases, even when the substrate CTE was changed. In general, the Young’s modulus increases as the volume fraction of glass cloth is increased to reduce a CTE [15]. It was observed from a supplementary numerical study, however, that the Young’s modulus of the substrate had virtually no effect on the warpage of the assembly. Accordingly, the Young’s modulus was not considered as a variable in the current parametric study.

The results in Table IV are plotted in Fig. 10, where the values were normalized by the reference case (a chip size of 11.94 mm, a substrate CTE of 17 ppm/°C and a substrate thickness of 0.76 mm). The results clearly indicate that the most critical parameter is the substrate CTE. The maximum strain increased most rapidly as the substrate CTE increased. Another noticeable trend was observed for the substrate thickness. For a given chip size and substrate CTE, the maximum strain also increased as the substrate thickness increased. The chip size did not affect the maximum solder strain as much as the other two parameters. However, it is interesting to note that, for a given substrate CTE and thickness, the maximum solder strain always occurred when the medium chip size (11.94 mm or 0.47 in) was used. After examining the strain components of the point of maximum strain, it was concluded that the combination of the curvature effect ($\varepsilon_z$) and the shear deformation ($\gamma_{yz}$) induced by the CTE mismatch between the chip shadow region and the PCB was the largest for the medium chip size.

In order to quantify the effect of the substrate CTE on the solder ball strain, the results in Table IV are re-plotted in Fig. 11 for each chip size. In each case of chip size, the maximum strains values were normalized by the value obtained from the case with the substrate CTE of 17 ppm/°C and the substrate thickness of 0.76 mm. The three different chip sizes of 6.96, 11.94 and 17.02 mm are plotted in (a), (b), and (c), respectively. Each plot

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**Table III**

<table>
<thead>
<tr>
<th>Variable</th>
<th>Chip size (mm)</th>
<th>Substrate CTE (ppm/°C)</th>
<th>Substrate thickness (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference case</td>
<td>11.94 (470 mil)</td>
<td>17</td>
<td>0.76 (30 mil)</td>
</tr>
<tr>
<td></td>
<td>17.02 (670 mil)</td>
<td>20</td>
<td>1.02 (40 mil)</td>
</tr>
</tbody>
</table>
As can be seen from all three plots, the maximum strain increased almost linearly as the CTE of the substrate increased. As the CTE increased, the curvature difference between the substrate and the PCB at the inflection point increased. This increased curvature difference was absorbed by the critical solder ball, which gave rise to a larger normal strains of $\varepsilon_z$.

As mentioned earlier, the maximum strain decreased slightly as the substrate thickness decreased. The bending stiffness of the substrate was reduced with a thinner substrate. As a result, the substrate became more compliant and reduced the magnitude of $\varepsilon_z$ at the inflection point. The magnitude of $\varepsilon_z$ would be very small if a flex substrate is used. When the substrate CTE was low, however, the curvature change at the inflection point became small, and thus the effect of the substrate thickness (or bending stiffness) became minimal for the same reason (Fig. 11).

IV. DISCUSSIONS

The results of the parametric study revealed that the curvature change in the substrate made a major contribution to the magnitude of the maximum strain of the critical solder ball. It also indicated that the size of the chip did not affect the solder strain, but the strain increased as the substrate thickness increased. This is distinctively different from the case of wire-bond plastic ball grid array (WB-PBGA) package assembly. It has been known that the solder ball reliability of WB-PBGA package assembly can be enhanced significantly by increasing the substrate thickness [16].

Fig. 12 represents the $V'$ or vertical displacement fields of two assemblies with similar dimensions. The assemblies were subjected to a uniform thermal loading of $\Delta T' = -60 \, ^{\circ}\text{C}$ and the

<table>
<thead>
<tr>
<th>Chip size (mm)</th>
<th>Substrate CTE (ppm/°C)</th>
<th>Substrate thickness (mm)</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>0.51 (20 mil)</td>
<td>0.76 (30 mil)</td>
</tr>
<tr>
<td>6.86 (270 mil)</td>
<td>14</td>
<td>0.09</td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>0.12</td>
</tr>
<tr>
<td></td>
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</tr>
<tr>
<td>11.94 (470 mil)</td>
<td>14</td>
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<td></td>
<td>17</td>
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<td>20</td>
<td>0.15</td>
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<tr>
<td>17.02 (670 mil)</td>
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<tr>
<td></td>
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<td>0.11</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>0.14</td>
</tr>
</tbody>
</table>

Fig. 10. Normalized maximum equivalent plastic strains.

contains three different substrate thicknesses of 0.51, 0.76, and 1.02 mm.
fringe patterns were obtained at room temperature by moiré interferometry [5], [17]. The distribution of the vertical displacement was determined from the fringe patterns using the following relationship [18]:

\[ V = \frac{1}{f} N_y \]  \hspace{1cm} (2)

where \( f \) is the frequency of the virtual reference grating (2400 lines/mm), and \( N_y \) are fringe orders in the \( V \) field moiré pattern. The displacements were extracted along the centerline of the substrate. The results are plotted in Fig. 12(b), where the \( V \) displacement and the \( x \) dimension were normalized by the maximum vertical displacement and the substrate width of each assembly, respectively. Note that the dimensions of the two assemblies were not identical but they were reasonably close for qualitative comparison.

As can be seen from Fig. 12(b), the deformed shapes of the substrates are distinctively different. In the WB-PBGA package assembly, the bare substrate region is covered with a high-modulus molding compound. As a result, the effective bending stiffness of the region becomes much larger and the substrate bends nearly uniformly without an inflection point at the edge of the chip. It is interesting to recall, however, that the maximum strain occurred at the solder ball located at the edge of the chip for both assemblies [5], [17]. This implies that the strain components that make the most significant contribution to the magnitude of the maximum EQPS should be different for the two package assemblies. Consequently, the design parameters optimized for en-

![Fig. 11. Maximum equivalent plastic strains normalized for each chip size: (a) 6.96 mm, (b) 11.94 mm, and (c) 17.02 mm.](image)

![Fig. 12. (a) V displacement fields of FC-PBGA package assembly and WB-PBGA package assembly induced by a thermal loading of \(-60 \, ^\circ\text{C}\) [5], [17] and (b) vertical displacements extracted along the centerline of the substrate. The contour interval in (a) is 0.417 \( \mu \text{m} \) per fringe.](image)
hanced solder ball reliability of WB-PBGA package assembly will not be always desirable for the optimum solder ball reliability of FC-PBGA package assembly, even when both assemblies have the identical chip, substrate and PCB.

V. CONCLUSION

An experimental investigation was conducted to document thermally-induced warpage of a FC-PBGA package and its assembly. The experimental results revealed that an inflection point in the substrate appeared at the edge of the chip. The appearance of the inflection point was ascribed to the different constraints from the chip and the PCB. An experimentally verified 3-D nonlinear FEA proceeded to quantify the effect of the substrate deformation on the solder ball strains. A parametric study was followed to identify the most critical design parameters for optimum solder joint reliability. The results indicated that the CTE of the substrate was most critical to the solder ball reliability. The results also indicated that the chip size did not affect the solder ball deformations significantly and the solder ball strain increased with a thicker substrate.

REFERENCES