Effect of Underfill on C4 Bumps and Surface Laminar Circuit: An Experimental Study by Microscopic Moiré Interferometry

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ABSTRACT

The effect of underfill on thermal deformations of the flip-chip PBGA package is investigated. Two experiments are conducted; one for the effect on C4 deformations and the other for effect on the surface laminar circuit. The packages are subjected to an isothermal loading and thermally induced displacement fields are documented by microscopic moiré interferometry. The ultra-high displacement measurement sensitivity and the microscopic spatial resolution of the method allow a detailed analysis within solder bumps and microstructures. The quantitative deformation data will be given and its implications on package reliability will be discussed.

Key words: C4, surface laminar circuit, underfill, micro moiré interferometry, flip-chip PBGA

Introduction

While the underfill innovation has made the flip chip on organic chip carrier a practical reality, the surface laminar circuit (SLC) innovation has enabled the PCB manufacturing infrastructure to produce laminate substrates with high density wires and fine pitch conductors required for advanced flip chip assemblies.

Extensive research and development efforts have been and are being made to perfect the underfill process for organic substrates, and to develop optimum underfill materials for the larger silicon devices. One of the most noticeable trends in newly developed underfill materials is its increased Young’s modulus. Although the other reliability issues such as adhesion, flowability, solder bump reliability, etc., have been improved, the coupling between the silicon chip and the substrate has also increased with the increased Young’s modulus. This high degree of coupling transfers the CTE mismatch induced loading to other interconnection layer.

This experimental investigation is intended to quantify the effect of the underfill on the deformations of (1) the C4 bumps of the direct chip attach (DCA) package and (2) the microstructures within the surface laminar layer of the SLC substrate.

Experimental Method: Microscopic Moiré Interferometry

The term microscopic moiré interferometry has been adopted for studies of local regions under high magnification [1]. Microscopic moiré interferometry is an extension of moiré interferometry but it is distinguished from conventional moiré interferometry by the need for higher spatial resolution and greater measurement sensitivity. The method employs an optical microscope for the required spatial resolution and enhances the sensitivity of moiré interferometry by an order of magnitude by utilizing an immersion interferometer and the optical/digital fringe multiplication (O/DFM) method. Microscopic moiré interferometry reveals fringe patterns of the U and V displacement fields, defined as in-plane displacements in orthogonal x and y directions, respectively. The displacements are determined from the contour maps by

\[ U = \frac{N_x^*}{\beta f}, \quad V = \frac{N_y^*}{\beta f} \]  

(1)

where \( N_x^* \) and \( N_y^* \) are contour numbers (proportional to fringe orders in the moiré patterns) in the two contour maps, respectively, and \( f \) is equal to 4800 lines/mm.
Specimen Preparation and Isothermal Loading

Microscopic moiré interferometry requires a plane of interest to be revealed and ground flat before specimen grating replication. The specimens were inserted in a precision vise and they were ground until the desired cross section was exposed as illustrated in Fig. 1. This specimen configuration maintained the three dimensional integrity of the specimen [2].

The specimens were subjected to an isothermal loading to determine steady-state thermal deformations. This was accomplished by transferring a uniform cross-line diffraction grating at an elevated temperature [3].

After the specimen was pried off from the grating mold, the specimen was cooled down to room temperature. The specimen deformed during cooling, and the specimen grating deformed together with it. The deformation was then recorded at room temperature by microscopic moiré interferometry. Thus, the moiré patterns obtained at room temperature represented the absolute change of deformations incurred during the isothermal loading.

Experiment I: Deformations of C4 bumps

The first experimental investigation is intended (1) to characterize the thermo-mechanical behavior of C4 bumps on an organic substrate and (2) to understand the effect of underfill on the deformations of C4 bumps.

Specimen Configuration

Two specimens were prepared for the experiments: two identical DCA packages, one without and the other with underfill. The specimens were subjected to an isothermal loading of ΔT = -60 °C to determine steady-state thermal deformations. The cross-sectional view of a flip chip package with underfill is shown in Fig. 1 with its relevant dimensions. In the package, a silicon chip (9.5 mm × 9.5 mm × 0.6 mm) was attached to a multi-layer FR4 PCB.

Experimental Results: Fringe Patterns

The grating mold used to replicate the specimen grating was made on an ultra low expansion (ULE) substrate. The ULE grating had virtually the same frequency over the temperature range of the experiment and it was used to tune a null field condition (devoid of fringes) of the microscopic moiré system. After achieving a null field by adjusting the angle of the fiber and adjusting in-plane rotation of the mold, the grating mold was replaced with the specimen containing the deformed grating. Then the deformations of each solder bump in the left half of the package were recorded while the interferometer was translated along the solder row of interest.

There were a total of 12 solder bumps in the half of the package. Figure 2 shows the U and V field patterns of two representative solder bumps (solder 3 and 9) of the package without underfill, where a fringe multiplication of 2 was used and the corresponding contour interval was 104 nm/contour. The numbers shown in the patterns denote the fringe order N. The large relative horizontal displacement between the top and bottom of the solder bumps is evident from the horizontal U field fringes in the solder bump. The U and V displacements of a solder bump (solder 12) of the package with underfill are shown in Fig. 3, where the region of the solder bump is marked by a solid line. A fringe multiplication of 4 was used and the corresponding contour interval was 52 nm/contour.

Analysis: Average Strain Distribution

Average normal and shear strains of solder bumps were evaluated from the displacement fields. The results are plotted in Fig. 4, where the insert illustrates the gage lengths used in the strain calculation. The result is striking. For the package without underfill, the average shear strain (γ_y^{ave}) increases linearly as the DNP increases. The magnitude of γ_y^{ave} of the solder 9 is about 2%, which is greater than that of the corresponding solder bump of the package with underfill by an order of magnitude. The effect of underfill is remarkable. The underfill reduced the average shear strain significantly and its magnitude remained nearly constant, independent of the DNP.

The average normal strain distributions (ε_y^{ave}) are plotted in Fig. 5. The magnitude of ε_y^{ave} is independent of the DNP and it is much smaller than γ_y^{ave} in magnitude. The ε_y^{ave} for the package without underfill was positive (tensile) while the ε_y^{ave} for the package with underfill was negative (compressive). The negative ε_y^{ave} was ascribed to the higher CTE of underfill material that contracted more
during cooling, producing a nominal compressive strain of solder bump.

The underfill material cures at an elevated temperature. As a result, this compressive strain would exist over the actual operating temperature of the package, which would help reduce the crack propagation at a low temperature. However, if this compressive stress relaxes at room temperature during storage, this mechanism would produce an undesired tensile strain of solder bump at an elevated temperature. This mechanism warrants more investigations and should be considered as an important selection parameter for underfill materials for optimum solder bump reliability.

Experiment II: Deformations of SLC

The results from the previous experiment indicated that the underfill encapsulant reduced the shear strain of the solder bumps significantly. However, the stresses produced by the CTE mismatch between the silicon device and the organic substrate do not disappear. Other microstructures must absorb the deformation caused by the CTE mismatch. The second experiment is intended to further investigate the effect of underfill on the deformation of microstructures within the surface laminar layer.

Specimen Configurations

Two specimens were prepared for this experiment; a bare SLC substrate, and a flip chip package on the identical substrate. They were subjected to an isothermal loading of $\Delta T = -70 ^\circ C$. The cross-sectional view of the flip chip assembly is illustrated schematically in Fig. 6 with its relevant dimensions. A silicon chip was 10 mm square attached to a SLC substrate with a BT core. The microstructures within the surface laminar layer are illustrated schematically in the insert of Fig. 6, where the thickness of surface laminar layer is 190 $\mu$m.

Experimental Results: Fringe Patterns

In order to understand the global behavior of the surface laminar layer, the deformation was first documented at a relatively large region of 900 $\mu$m by 675 $\mu$m. Figure 7 depicts the location and the micrograph of the region obtained before application of the specimen grating. The U and V displacement fields obtained from the two specimens are shown in Fig. 8 for (a) the bare substrate and (b) the flip chip assembly, where a fringe multiplication of $\beta = 2$ was used and the corresponding contour interval was 104 nm/fringe contour.

For the more detailed deformation analysis within the surface laminar layer, the displacement fields were captured for a smaller region containing the microstructures. The region is marked by a dashed box in Fig. 7 and it is 500 $\mu$m by 375 $\mu$m. The resultant fringe patterns are shown in Fig. 9 for (a) the bare substrate and (b) the flip chip assembly. The higher displacement sensitivity was required to increase the number of fringes in the smaller field of view. For the patterns shown in Fig. 9, a fringe multiplication factor of $\beta = 4$ was used to produce a displacement contour interval of 52 nm/fringe.

Analysis

Photosensitive Dielectric Layer

The surface laminar layer in the bare substrate shows a uniform contraction in the x and y directions but with a higher rate in the y direction. The deformation of the relatively soft photosensitive dielectric layer was constrained by the BT core in the x direction and it deformed together with the core. The photosensitive material has a much higher CTE value ($\approx 70$ ppm/$^\circ C$) than the core ($\approx 17$ ppm/$^\circ C$). As a result, the total deformation of the layer in the x direction was smaller than the free thermal contraction, as can be seen from the sparse U field fringes in the layer (Fig. 8a). This constraint produced a stress-induced tensile strain ($\sigma \varepsilon_x$) in the layer. In the direction perpendicular to the layer, however, the constraint from the core did not exist. The surface laminar layer deformed freely in the y direction, resulting in the densely spaced horizontal fringes in the layer (V field in Fig. 8a).

In the flip chip assembly, the deformation of the surface laminar layer was also constrained by the chip through the coupling of the underfill. The CTE of the chip (3 ppm/$^\circ C$) is much lower than the CTE of the core. In addition, most of the constraint from the chip is transferred to the surface laminar layer because of the high modulus of underfill. Consequently, the degree of the constraint in the top and the bottom of the layer is different. This non-uniform constraint produced the relative horizontal displacements between the top and the bottom of the layer. The average shear strain of the layer was evaluated from the fringe patterns in Fig. 8b and the result is plotted in Fig. 10. The DNP-dependent shear strain is evident.

The strain distributions through the thickness of the photosensitive dielectric layer (AA') are plotted in
As mentioned earlier, the constraint in the x direction produced a positive $\varepsilon_x^o$ in the surface laminar layer. The magnitude of $\varepsilon_x^o$ increased after the flip chip/underfill process that produced the extra constraint from the chip. The maximum $\varepsilon_x^o$ of the layer in the flip chip assembly occurred at the interface with the metal via and its magnitude was about 0.48%.

For the bare substrate, the in-plane shear strain $\gamma_{xy}$ of the layer was zero as expected from the uniform constraint in the x direction and the free contraction in the y direction. The magnitude of $\gamma_{xy}$ increased again after the flip chip/underfill process as a result of the different degree of constraint in the top and the bottom of the layer. The magnitude was nearly uniform through the thickness and its maximum value was about 0.33% at the interface with the metal via.

The most interesting result was observed in the distribution of $\varepsilon_y^o$. The magnitude of $\varepsilon_y^o$ for the bare substrate was small near the free surface and it increased almost linearly through the thickness. The increase of $\varepsilon_y^o$ was ascribed to the Poisson’s effect and the constraint from the metal traces imbedded in the layer. A similar trend of $\varepsilon_y^o$ distribution was observed for the flip chip assembly but the magnitude of $\varepsilon_y^o$ increased significantly with the underfill. The magnitude of the maximum $\varepsilon_y^o$ was -0.92%. This large increase of $\varepsilon_y^o$ was caused by the bending of the assembly as well as the Poisson’s effect.

The strain distributions along the solder resist mask (BB’) are plotted in Fig. 12. They represent the average strains of the solder resist mask. The magnitude of $\varepsilon_x^o$ increased with the flip chip/underfill process and remained nearly constant along BB’ The maximum value of $\varepsilon_x^o$ is about 0.38% that is slightly lower than half the typical tensile strength of the solder resist mask.

The magnitude of $\varepsilon_y^o$ and $\gamma_{xy}$ was small for the bare substrate. However, the distribution and the magnitude of $\varepsilon_y^o$ and $\gamma_{xy}$ were changed significantly by the flip chip/underfill process. The magnitude of $\varepsilon_y^o$ was small and negative at the interface with the solder (Point B). Its magnitude increased rapidly to its peak value of -0.67% and decreased gradually along BB’. Similar to $\varepsilon_y^o$, the shear strain was also small and negative at the interface with the solder, but it increased quickly to its positive peak value. The peak value of $\gamma_{xy}$ was 0.48%.

**Conclusions**

Microscopic moiré interferometry was employed to document the effect of underfill on thermal deformations of (1) C4 bump and (2) microstructures in the surface laminar layer. The specimens were subjected to an isothermal loading. The nano scale displacement sensitivity and the microscopic spatial resolution of the method delineated clearly the complex deformation of the C4 bumps and the microstructures embedded in the surface laminar layer. The underfill reduced the shear strains of the C4 bumps by more than an order of magnitude. However, the extra constraint from the chip through a high degree of coupling provided by the underfill produced the significant deformation within the surface laminar layer that increased proportionally to the DNP. This deformation is expected to increase proportionally with the larger silicon devices. It is suggested that the underfill strength be optimized not only for the solder bump reliability but also for the system reliability, taking deformations of other microstructures into consideration.

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**References**

Fig. 1 Schematic diagram of DCA package without underfill; (a) before and (b) after specimen preparation.

Fig. 2 U and V displacement fields of two representative solder bumps of the package without underfill. The contour interval is 104 nm per fringe.

Fig. 3 U and V displacement fields of solder bump 12 of the package with underfill. The contour interval is 52 nm per fringe.

Fig. 4 Average shear strain ($\gamma_{xy}^{\text{ave}}$) distributions.

Fig. 5 Average normal strain ($\varepsilon_y^{\text{ave}}$) distributions.

Fig. 6 Schematic diagram of the flip chip assembly on the SLC substrate; (a) before and (b) after specimen preparation.

Fig. 7 Micrographs of the region of interest.
Fig. 8  Microscopic U and V displacement fields of the region of interest shown in Fig. 3; (a) bare substrate and (b) flip chip assembly. The contour interval is 104 nm per fringe.

Fig. 9  Microscopic U and V displacement fields of the region, marked by the dashed box in Fig. 3, with a higher sensitivity; (a) bare substrate and (b) flip chip assembly. The contour interval is 52 nm per fringe.

Fig. 10  Average shear strain distribution as a function of DNP.

Fig. 11  Stress-induced strain distributions through the thickness of the photosensitive dielectric layer (AA’).

Fig. 12  Stress-induced strain distributions along the solder resist mask (AA’).