Effect Of Underfill On Flip-Chip Solder Bumps: An Experimental Study By Microscopic Moiré Interferometry

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Abstract

Thermo-mechanical deformations of flip-chip interconnections on an organic substrate are investigated by microscopic moiré interferometry. A detailed experimental procedure for microscopic moiré experiments is described and the effect of specimen preparation is discussed. Two identical packages—one without and the other with underfill—are investigated. They are subjected to a uniform thermal loading and thermally induced displacement fields are documented by microscopic moiré interferometry. The ultra-high displacement measurement sensitivity and the microscopic spatial resolution of the method allow a detailed analysis of solder bumps. The normal and shear strains (averaged along the vertical centerlines) at each solder bump are calculated from the displacement fields. The experimental results confirms the effect of underfill on the solder bump strains; the average shear strains are reduced by an order of magnitude and the average normal strains in the direction perpendicular to the chip thickness becomes compressive.

Key words:
Flip chip, Underfill, Organic substrate, Microscopic moiré interferometry, Thermal strains, Global CTE mismatch, Local CTE mismatch

Introduction

The flip chip technology has emerged as an important future chip technology to meet ever-increasing demand of high I/O requirement. In conventional packages, such as wire bonding and tape automated bonding, the chip is positioned on its back surface and small diameter wires are used to connect the bonding pads located around the perimeter of the chip surface to the chip carrier. In chip carriers using flip chip connections, this conventional orientation of the chip is reversed. The chip is placed face downward and the connection between the chip and the chip carrier is achieved by a solder bump. Because of this orientation, the flip chip package has numerous advantages over the conventional packages. They include (1) substrate space efficiency (higher I/O capacity) from the area array configuration, (2) better electrical performance from low capacitance and inductance of small
joint size and (3) enhanced thermal performance; the top surface of the chip is available for direct heat sink attachment, etc. (Lau, 1994).

The flip chip technology was implemented originally for the multi-layer ceramic substrate. In the ceramic flip chip package, the dominant deformation of solder bumps was shear strains produced by the mismatch of coefficient of thermal expansion (CTE) between the chip and the ceramic substrate. The average shear strain in each bump was proportional to its distance from the neutral point (DNP). Consequently, the size of silicon device was limited to prevent solder bumps from premature failure.

Recently, the innovative underfill technique has been developed and implemented for the flip chip technology, where the gaps between the solder bumps are filled with an epoxy encapsulant. The underfill technique improved the thermal fatigue life of solder bumps significantly to allow use of larger silicon devices on a ceramic substrate. This remarkable improvement of solder fatigue provided by the underfill enabled the industry to extend the flip chip technology to organic substrates, although deformations caused by the thermal expansion mismatch were much exacerbated because of the higher CTE of organic substrates (Tsukada, et al., 1992). Extensive research and development efforts are being performed to develop new underfill materials for the larger silicon devices as predicted in National Technology Roadmap for Semiconductors (SIA, 1997).

This experimental investigation is intended (1) to characterize the thermo-mechanical behavior of solder bumps on an organic substrate and (2) to understand the effect of underfill on the deformations of solder bumps. Detailed thermal deformations within a solder bump are required. Use of an experimental method with extremely high displacement measurement sensitivity and a high spatial resolution is inevitable. Moiré interferometry has been used extensively for thermal deformation analyses of microelectronics devices (Bastawros and Voloshin, 1990; Guo et al., 1993; Han and Guo, 1995). The sensitivity of moiré interferometry, however, is not sufficient for a tiny structure of current interest. Within such a small structure, the relative displacements can be small even when the strains are large. Accordingly, higher sensitivity is needed to obtain enough fringes to effectively map the displacement field. Microscopic moiré interferometry was developed for this need for enhanced displacement measurement sensitivity and microscopic spatial resolution [Han, 1992 and Post et al., 1994]. It has been applied for thermal deformations of interconnections in microelectronic subassemblies [Han and Guo, 1995].

Moiré interferometry and microscopic moiré interferometry have been matured in the last decade. Moiré interferometry is routinely practiced in numerous industry laboratories. Yet, practice of microscopic moiré interferometry has been limited because of complexity involved in the experimentation. The objective of this paper is (1) to provide a detailed experimental procedure of microscopic moiré experiments when it is applied for thermal deformation analysis of solder interconnections and (2) to report experimental data and the resultant strain distributions of flip-chip solder bumps. The effect of specimen preparation on measured displacements is also discussed.

**Background: Microscopic moiré Interferometry**

Special considerations arise for deformation measurements of tiny specimens or tiny regions of larger specimens. The relative displacements within a microscopic field of view will be small (even if the strains are not small), so the number of moiré fringes might not be enough for an accurate analysis. Perhaps the most important consideration, therefore, is the need for increased displacement sensitivity and microscopic spatial resolution. Microscopic moiré interferometry is an extension of moiré interferometry (Post et al., 1994) but it should be distinguished from conventional moiré interferometry by the need for higher spatial resolution and greater measurement sensitivity.
In microscopic moiré interferometry, sensitivity is increased progressively by two techniques. The first is an immersion interferometer, whereby the virtual reference grating is formed inside a medium of higher index of refraction; this strategy reduces the wavelength of the light and thus increases the upper limit of frequency for the virtual reference grating. Virtual reference gratings of 4800 lines/mm are produced in practice, thus doubling the usual basic sensitivity of moiré interferometry [Han, 1992 and Post et al, 1994]. The second technique is optical/digital fringe multiplication (O/DFM), whereby fringe shifting and an efficient algorithm is used to generate an enhanced contour map of the displacement field; the map displays $\beta$ times as many fringe contours as the original moiré pattern [Han, 1993]. In practice, $\beta = 12$ has been achieved for microscopic moiré interferometry, which with the doubled sensitivity of moiré interferometry, represents a multiplication of 24.

A specific system used by the authors will be described briefly. The technique is described in much more detail in the reference [Post et al, 1994]. It is based on the premise that the moiré pattern encompassing the small field of view will contain only a few fringes. Accordingly, it is practical to record the pattern by a CCD camera. Good fringe resolution is preserved because the pattern is recorded with numerous pixels per fringe.

The apparatus is illustrated in Fig. 1. The specimen is coupled optically to the interferometer by a thin layer of immersion fluid, so that four beams required for two orthogonal displacement fields propagate in a refractive medium. A magnified view of the fringe pattern is recorded by the CCD camera, which digitizes the intensity level at every pixel. A piezoelectric translation device provides the means for phase stepping. The entire system is moved relative to the specimen by the $xy$ traverse, allowing any part of the specimen to be viewed and analyzed.

The result is a fringe contour map of ultra-high sensitivity covering the measurement zone. The displacements are determined from the contour maps by

$$U = \frac{N_x^*}{\beta f}, \quad V = \frac{N_y^*}{\beta f} \tag{1}$$

Where $N_x^*$ and $N_y^*$ are contour numbers in the two contour maps, $f$ is the frequency of the virtual reference grating, and $\beta$ is a fringe multiplication factor.

In those cases, where strains are calculated from the measured displacement fields, they are determined by the small-strain relationships

$$\varepsilon_x = \frac{\partial U}{\partial x} = \frac{1}{f} \left[ \frac{\partial N_x}{\partial x} \right], \quad \varepsilon_y = \frac{\partial V}{\partial y} = \frac{1}{f} \left[ \frac{\partial N_y}{\partial y} \right]$$

$$\gamma_{xy} = \frac{\partial U}{\partial y} + \frac{\partial V}{\partial x} = \frac{1}{f} \left[ \frac{\partial N_x}{\partial y} + \frac{\partial N_y}{\partial x} \right] \tag{2}$$

**Specimen preparation**

A flip chip package used in the experiment is illustrated schematically in Fig. 2a with its relevant dimensions. In the package, a silicon chip (9.5 mm x 9.5 mm x 0.6 mm) was attached to an organic substrate by solder bumps. The substrate was a multi-layer FR4 printed circuit board (PCB) and its thickness was 1.55 mm. The typical height of solder bumps was 100 $\mu$m.
Two specimens were prepared for the experiments: two identical flip-chip packages, one without and the other with underfill. Microscopic moiré interferometry requires a plane of interest to be revealed and ground flat before specimen grating replication. A single package was trimmed from a fully populated PCB by using a medium speed diamond saw with a high concentration blade [Model 8000, Lapcraft] and a low speed high precision diamond saw [Isomet, Buehler Co.]. The trimmed package was inserted in a precision vise with the package side facing a movable jaw, as illustrated in Fig. 2b. The position of the package was adjusted under a low magnification stereomicroscope until a desired cross section is aligned with the side of the vice under a stereomicroscope. Then, the specimen was ground by setting the vise onto a variable speed grinding wheel with a fine grit grinding paper (typically 600 to 1200 grit) until a solder row along the edge of chip was exposed as shown in Fig. 2c. The vice was made of hardened carbon steel and the square edges of the vice ensured a flat and square surface of the specimen after grinding.

Thermal loading

The packages were subjected to a uniform thermal loading to determine steady-state deformations. This was accomplished by transferring a uniform cross-line diffraction specimen grating at an elevated temperature (Post and Wood, 1989). A special grating replication technique (Guo et al., 1993) was used for the package without underfill to produce a very clean edge of the cross section after grating replication. The clean edge was critical since the excess epoxy could reinforce the specimen and change the local strain distribution.

After the specimen was pried off from the grating mold at the elevated temperature (T₁), the specimen was cooled to room temperature (T₀). The specimen deformed during cooling, and the specimen grating deformed together with it. The deformation was then recorded at room temperature by microscopic moiré interferometry. Thus, the deformation induced by the change of temperature (ΔT = T₁ − T₀) was documented.

This procedure is very effective when deformation incurred between two reference temperatures is sought. It measures the deformation that occurs in the interval between the application of the specimen grating and the subsequent observation of the deformed grating. Since the measurements are independent of any previous state of deformation, the effect of process variables such as underfill can be assessed accurately by directly comparing the
data obtained from the identical thermal excursion.

This technique has come to be known as isothermal loading in recent years, but that name implies constant temperature and therefore it is not descriptive. We propose to call the technique bithermal loading, implying two discrete temperatures.

**Experimental procedure and fringe patterns**

The grating mold used to replicate the specimen grating was made on an ultra low expansion (ULE) substrate. The ULE grating had virtually the same frequency over the temperature range of the experiment and it was used to tune a null field condition (devoid of fringes) of the microscopic moiré system. After achieving a null field by adjusting the angle of the fiber and adjusting in-plane rotation of the mold, the grating mold was replaced with the specimen containing the deformed grating. Then the deformations of each solder bump in the left half of the package were recorded while the interferometer was translated along the solder row of interest.

It is important to note that the distance between the specimen surface and the microscope lens must be maintained in order to avoid carrier patterns of extension that would add undesired normal gradients to the displacement fields. It was achieved during the experiment by the following procedure; (1) the microscope was adjusted to provide a good focus over the region on the ULE grating and (2) when the specimen was replaced and the specimen image lost its focus, the position of the specimen holder was adjusted to regain the focus across the entire field. This procedure ensured that the specimen grating was in essentially the same plane as the grating on the ULE.

There were a total of 12 solder bumps in the half of the package. Figure 3 shows the U and V field patterns of two representative solder bumps (solder 3 and 9) of the package without underfill, subjected to a thermal loading of $\Delta T = -60^\circ C$.

The insert in Fig. 3 shows the micrographs of the corresponding solder bumps and the boundaries of the microstructures are marked in the fringe patterns. A fringe multiplication of 2 was used for the experiments and the corresponding contour interval was 104 nm/contour. The numbers shown in the patterns denote the fringe order $N^*$. In spite of an extreme care given during replication, the epoxy extended beyond the boundaries of the solder bumps. Debris of solder was produced during grinding. It was stick to the boundaries of solder bumps and the epoxy covered it during replications. The debris was not mechanically connected to the solder bumps and its reinforcing effect was not significant. The following experimental observation supports the speculation.

The large relative horizontal displacement between the top and bottom of the solder bumps is evident from the horizontal U field fringes in the solder bump. The U field pattern shows...
nearly uniform negative gradient of \( \frac{\partial U}{\partial y} \) in the solder bump. However, the V field shows a non-uniform positive gradient of \( \frac{\partial V}{\partial x} \) in the solder bump. At the free edge, the companion gradients of \( \frac{\partial U}{\partial y} \) and \( \frac{\partial V}{\partial x} \) for shear strain are equal in magnitude and opposite in sign. They cancel to yield zero shear strain. The experimental data are consistent with the requirement that the shear stress (and shear strain) must vanish at the free edge.

Engineering strains are determined from the displacement gradient, which requires differentiation of displacement field. For shear strains, the displacement gradients in the x and y directions are required. Another sets of fringe patterns were documented after applying carrier patterns of rotation to increase accuracy in data reduction. The carrier patterns were applied by rotating the specimen with respect to the optical system. The amount of carrier pattern was adjusted until the cross derivative of the V displacement \( \frac{\partial V}{\partial x} \) became nearly zero in the central portion of each solder bump. The resultant patterns of solder 9 are shown in Fig. 4. Note that the carrier patterns of rotation altered the displacement fields but the magnitude of normal and shear strains remained unchanged (Post et al., 1994).

The U and V displacements of two representative solder bumps (solder 6 and 12) of the package with underfill subjected to an identical thermal loading of \( \Delta T = -60^\circ C \) are shown in Fig. 5, where the region of each solder bump is marked by a solid line. A fringe multiplication of 4 was used for the experiment and the corresponding contour interval was 52 nm/contour. As expected, the underfill produces a strong coupling between the chip and the substrate. This coupling produces a substantial bending deformation of the assembly. Unlike the package without underfill, the large negative shear gradient \( \frac{\partial U}{\partial y} \) shown in the U displacement field was not caused by the shear strain. Instead, it represents the rigid-body displacement induced by the bending of the package. Note that the shear gradient \( \frac{\partial V}{\partial x} \) in the V displacement field is also large but opposite in sign. This rigid-body rotation was nullified by rotating the specimen until the shear...
gradient \( \frac{\partial V}{\partial X} \) became essentially zero. The resultant patterns of solder 12 after canceling the rigid body displacement are shown in Fig. 6.

Fig. 6. U and V displacement fields of solder 12 of the package with underfill after canceling rigid body rotation. The contour interval is 52 nm per fringe.

The presence of underfill significantly altered the deformation of solder bumps. With the underfill, the discrete solder bump structure was transformed into a continuous layer, which reduced the shear displacements significantly. In addition, the free edge does not exist and the V displacement field is much more uniform compared to the package without underfill.

Analysis and results

Average strain distribution (Effect of global CTE mismatch)

Average normal and shear strains of solder bumps were evaluated from the displacement fields by using the following relationship;

\[
\varepsilon_y^{\text{ave}} = \frac{1}{\beta f} \left( \frac{\Delta N_x}{\Delta y} \right) - \varepsilon^\alpha = \frac{1}{\beta f} \left( \frac{\Delta N_x}{\Delta y} \right) - \alpha \Delta T
\]

\[
\gamma_{xy}^{\text{ave}} = \frac{1}{\beta f} \left( \frac{\Delta N_x}{\Delta y} + \frac{\Delta N_y}{\Delta x} \right)
\]

where \( \Delta x \) and \( \Delta y \) are the width and height of solder bump, respectively; \( \Delta N_x \) and \( \Delta N_y \) are a number of fringes across the corresponding gage length; \( \varepsilon^\alpha \) is the strain induced by a free thermal contraction; \( \alpha \) is a coefficient of thermal expansion of solder (21 ppm/°C); and \( \Delta T \) is a temperature change in the isothermal loading (-60°C). Note that a free thermal contraction does not affect the magnitude of \( \gamma_{xy} \). The average normal strains in the x direction are much smaller in magnitude and they are not reported here.

The average shear strain distributions are plotted in Fig. 7, where the insert illustrates the gage lengths used in the strain calculation. The result is striking. For the package without underfill, the average shear strain \( (\gamma_{xy}^{\text{ave}}) \) increases linearly as the DNP increases. The magnitude of \( \gamma_{xy}^{\text{ave}} \) of the solder 9 is about 2%, which is greater than that of the corresponding solder bump of the package with underfill by an order of magnitude. The effect of underfill is remarkable. The underfill reduced the average shear strain significantly and its magnitude remained constant, independent of the DNP.

The deformation of solder bump of the package without underfill can be explained further from the deformed shape of a solder bump. The deformed shape of the solder 9 was obtained from the fringe patterns shown in Fig. 3. The fringe patterns were marked at uniform intervals along the solder boundary and the (fractional) fringe orders were determined at each mark. Then, Fig. 8 was plotted by displacing each...
boundary point by an amount proportional to the U and V fringe orders. The deformations in Fig. 8 are greatly exaggerated. The deformed shape clearly indicates that the solder bump underwent nearly pure shear deformation in spite of the low stiffness of the organic substrate.

![Deformed shape of solder 9 of the package without underfill.](image)

This shear dominant deformation is changed into the bending dominant deformation after the underfill encapsulant fills the gap between the solder bumps. Prior to the micro moiré experiments, the bending (or out-of-plane) displacements of the packages were documented at room temperature by Far Infrared Fizeau Interferometry (FIFI). The FIFI produces surface contours of dielectric rough surface with a contour interval of 5.3 µm/fringe (Verma et al., 1999). The fringe patterns obtained from the packages are shown in Fig. 9a. The fringe patterns represent the warpage of the chip at room temperature, induced by cooling the packages from the assembly temperature. The chip in the package without underfill is flat at room temperature. The CTE mismatch between the chip and the substrate was absorbed by the shear deformations of the soft solder bumps. However, the chip in the package with underfill reports a significant bending. It was ascribed to a high degree of coupling between the chip and the substrate produced by the underfill layer. The bending displacements of the chip were evaluated along a diagonal line DD' and the results are plotted in Fig. 9b. The maximum relative out-of-plane displacement between the center and the edge of the chip was 26.5 µm. This large bending displacement reduced the relative horizontal displacement between the top and the bottom of the solder bump and thus decreased the average shear strains.

![Warpage contour of the chips obtained by FIFI, where the contour interval is 5.3 µm per fringe and (b) W displacements of the chip in the package with underfill along DD'.](image)

The average normal strain distributions ($\varepsilon_{y}^{ave}$) are plotted in Fig. 10. The magnitude of $\varepsilon_{y}^{ave}$ is independent of the DNP and it is much smaller than $\gamma_{xy}^{ave}$ in magnitude. The positive $\varepsilon_{y}^{ave}$ for the package without underfill can be induced from the deformed shape of Fig. 8. The large relative horizontal displacement between the top and bottom of solder bump occurred but the top and bottom planes were not allowed to rotate due to the rigid constraints of the chip and the substrate. This constraint produced positive $\varepsilon_{y}^{ave}$ in the solder bump. On the contrary, $\varepsilon_{y}^{ave}$ for the package with underfill was compressive.
It is ascribed to the higher CTE of underfill material that contracts more during cooling, producing a nominal compressive strain of solder bump.

The underfill material cures at an elevated temperature. As a result, this compressive strain would exist over the actual operating temperature of the package, which would help reduce the crack propagation at a low temperature. However, if this compressive stress relaxes at room temperature during storage, this mechanism would produce an undesired tensile strain of solder bump at an elevated temperature. This mechanism warrants more investigations and should be considered as an important selection parameter for underfill materials for optimum solder bump reliability.

Effect of local CTE mismatch
The shear strains within the solder bump of the package without underfill were investigated further to provide a better understanding of the effect of local CTE mismatch (CTE mismatch between the solder bump and the chip at the interface). The shear strains of solder 9 were calculated along two horizontal lines as illustrated in the insert of Fig. 11; AA’ along the interface between the chip and solder bump and BB’ along the centerline of solder bump. The results are shown in Fig. 11, where the shear strains are normalized by the maximum value.

At the chip/solder interface, the local CTE mismatch is present since the CTE of solder material is much larger than that of the chip. The effect of local CTE mismatch is zero at the center of the solder bump (r = 0) and the effect increases as r increases. It is important to note that the effect of the local CTE mismatch on the shear strains is not always additive. The local CTE mismatch has an additive effect at the left corner of the chip/solder interface, while it has a subtractive effect at the right corner of the same interface (Guo et al., 1993).

This local CTE effect is evident in Fig. 11. Along the line BB’, the shear strain distribution was almost symmetric and the maximum strain occurred near r = 0. Along the line AA’, however, the maximum shear strain did not occur at the middle of the solder bump. Instead the location was shifted toward the corner with the additive effect. For the large solder ball (≈
800 µm) of the ceramic ball grid array (CBGA) package assembly, the magnitude of the shear strain induced by the local CTE mismatch was approximately the same as that induced by the global CTE mismatch [Guo et al., 1993]. However, the effect of the local CTE mismatch was not significant for the small solder bump investigated in this study.

**Effect of specimen preparation**

In the moiré experiments, the plane of interest of the specimen was revealed and ground flat before specimen grating replication (Fig. 2). This specimen preparation would change the loading and geometric boundary conditions of the assembly. A supplementary experimental and numerical analysis was conducted to evaluate the effect.

![Moiré images](image)

(a) Warpage contour of the chips obtained by FIFI, where the contour interval is 5.3 µm per fringe and (b) W displacements of the chip in the package with underfill along DD'.

The warpage of the chip is directly related to the global loading condition. The change of warpage caused by specimen preparation was investigated. The fringe patterns shown in Fig. 12a were obtained by the FIFI after specimen preparation. As expected, the chip in the package without underfill remained flat after specimen preparation. For the package with underfill, the bending displacements of the chip obtained from Fig. 12a (after specimen preparation) are compared with those obtained from Fig. 9a (before specimen preparation). As can be seen in Fig. 12b, the warpage change caused by specimen preparation was not significant (less than 5%). This configuration maintains three-dimensional mechanical integrity of the specimen. The fringe patterns confirm the results of the previous numerical study that the change in the global loading condition was minimal for the specimen configuration shown in Fig. 2c (Han et al., 1995).

![Strain distribution](image)

Fig. 13. Average normal strain ($\varepsilon_{ave}$) distributions.

It is also important to note that the surface of the solder bump becomes traction-free after specimen preparation. This modified boundary condition would redistribute the stresses over the remaining half of the solder bump, especially for the solder bumps in the package without underfill. A 3-D finite element analysis was conducted to quantify the effect. The 3-D model simulating the package before specimen preparation (referring to Fig. 2a) is shown in Fig. 13a, where quarter symmetry is employed to represent the whole package. The corresponding 3-D model simulating the package after specimen preparation (referring to Fig. 2b) is shown in Fig. 13b, where half symmetry is employed and a traction-free boundary condition is imposed on the sectioned
plane. The models were subjected to an identical thermal loading. Figure 14 plots the deformed shape of the solder bump with the largest DNP in the xy plane. The deformed shapes are nearly identical. The shape change of solder bump does not affect its deformed mode significantly.

The above analysis indicates that the experimental data presented in this study reflect the actual deformation mechanism of the solder bump in spite of the modifications of specimen configuration required for moiré experiments.

Conclusions

Microscopic moiré interferometry was employed to document thermo-mechanical deformations of solder bumps on an organic substrate. Two identical flip chip packages—one without and the other with underfill—were subjected to an isothermal loading of $\Delta T = -60^\circ C$ and thermal deformations were documented at room temperature. The ultra high sensitivity and the microscopic spatial resolution of the method provided a faithful account of the in-plane displacements within the tiny solder bumps. The stress-induced strains were evaluated from the displacement fields. The presence of underfill significantly reduced the shear strains of solder bumps that otherwise were linearly proportional to the DNP. The effect of the local CTE mismatch was also investigated. The effect of the local CTE mismatch was not as significant as reported in the solder ball of the CBGA package assembly.

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